Top Digital Electronics Questions

Q.1	**Do as directed:**		
	1.	$(516)_7$ = ( )$_{10}$= ( )$_{16}$	
	2.	$(250.5)_{10}$ = ( )$_8$= ( )$_4$	
	3.	$(2ED)_{16}$=( )$_8$=( )$_2$	
	4.	$(38)_9$=( )$_5$=( )$_2$	
	5.	Obtain the 9's and 10's complement of $(864)_{10}$.	
Q.2	**Do as directed:**		
	1.	$(198)_{12}$+$(12121)_3$=( )$_8$	
	2.	Determine the value of base x if $(50)_x$=$(203)_4$	
	3.	Given the two binary numbers X = 1010101 and Y = 1001011, perform the subtraction X-Y using 1's complements.	
	4.	Using 10's complement perform $(4572)_{10}$-$(2102)_{10}$.	
	5.	Multiply the $(135)_6$ and $(43)_6$ in the given base without converting to decimal.	
Q.3	**Do as directed:**		
	1.	$(347)_{10}$ = ( )$_2$= ( )$_8$= ( )$_5$ = ( )$_{16}$ = ( )$_{BCD}$	
	2.	$(11010111.110)_2$ = ( )$_{10}$= ( )$_{12}$= ( )$_{16}$	
	3.	Obtain the 9's and 10's complement of $(389.61)_{10}$.	
Q-4	**Do as directed:**		
	1.	Multiply the $(267)_8$ and $(71)_8$ in the given base without converting to decimal.	
	2.	$(103)_4$ + $(50)_7$ = ( )$_9$	
	3.	Determine the value of base b if $(211)_b$=$(152)_8$	
	4.	Given the two binary numbers X = 11010 and Y = 1101, perform the subtraction X-Y using 2's complement.	
	5.	Using 9's complement perform $(582)_{10}$-$(1002)_{10}$.	
Q.5	**(a)**	Define duality principal and explain it with the help of example. Find the complements of the functions **F1 = x'yz' + x'y'z** and **F2 = x(y'z'+yz)** by taking their duals and complementing each literal.	
	(b)	Demonstrate by means of truth tables the validity of the De Morgan's theorems for three variables. Find the complement of **F = a(b'c'+bc)** by applying De Morgan's theorem as many times as necessary.	
Q.6	**(a)**	Demonstrate by means of truth table the validity of the distributive law of + over ·. Also show that the NOR and NAND operators are not associative.	
	(b)	Prove that a positive-logic AND gate is a negative-logic OR gate and vice-versa.	
Q.7	**(a)**	Express the Boolean function **F(p, q, r, s)=s(p'+q)+q's** in a sum of minterms and a product of maxterms.	
	(b)	Given the Boolean function: **F=xy+x'y'+y'z**	
		1.	Implement it with *only* OR and NOT gates.
		2.	Implement it with *only* AND and NOT gates.
Q.8	**(a)**	What is the difference between canonical form and standard form? Express the Boolean function **F(p, q, r)=(pq+r)(q+pr)** in a sum of minterms and a product of maxterms.	
	(b)	Realize 2 input X-OR gate using NOR gates only.	
Q.9	**(a)**	Simplify the following Boolean expressions by manipulation of Boolean algebra.	
		1.	F(x,y,z)=xy+xyz+xyz'+x'yz
		2.	F(A,B,C,D)=A'C(A'BD)'+A'BC'D'+AB'C

	(b)	Simplify the Boolean function **F(w,x,y,z)=w'x'z'+w'yz+w'xy** using don't care conditions **d=w'xy'z+wyz+wx'z'** in (i) sum of products and (ii) product of sums using Karnaugh map.	
Q.10	**(a)**	Prove that:	
		1.	wx+x'y+wy=wx+x'y
		2.	(AB+C+D)(C'+D)(C'+D+E)=ABC'+D
		3.	(A+B)'(A'+B')'=0
	(b)	Simplify the function F(A,B,C,D,E)=Σm(0,2,4,6,9,11,13,15,17,21,25,27,29,31) using Karnaugh map.	
Q.11	**(a)**	Reduce the following Boolean expressions to the required number of literals.	
		1.	F(A,B,C,D)=(A+C+D)(A+C+D')(A+C'+D)(A+B') to four literals.
		2.	F(w,x,y,z) = [(yz)'+w]'+w+yz+wx to three literals
	(b)	Simplify the Boolean functions F= w'(x'y + x'y'+ xyz) +x'z' (y+w) using don't-care conditions d=w'x (y'z + yz') + wyz in (i) sum of products and (ii) product of sums using Karnaugh map.	
Q.12	**(a)**	Simplify the following Boolean expressions.	
		1.	F(w,x,y,z) = xy+wy'+wx+xyz
		2.	F(p, q, r, s) = (p'+q) (p+q+s)s'
	(b)	Simplify the following Boolean functions using Karnaugh map:	
		1.	F(A,B,C,D)=Π(0,1,2,3,4,10,11)
		2.	F(w,x,y,z)=Σm(0,1,2,4,5,12,13,14) + don't care conditions Σd(6,8,9).
Q.13	**Write brief notes on:**		
	(a)	Full adder	
	(b)	Read-Only Memory (ROM)	
Q-14	**(a)**	Why are NAND and NOR gates known as universal gates? Explain in detail.	
	(b)	Explain full- subtractor. Implement a full-subtractor with two half- subtractors and an OR gate.	
Q.15	Implement Boolean functions		
	(a)	F= (A +B') (CD+E) using only NAND gates.	
	(b)	F=A (B+CD) +BC' with only NOR gates.	
	(c)	F=x'y+xy' using only four NAND gates.	
Q.16	Simplify the function F(w,x,y,z)=Σ(0,1,2,8,10,11,14,15) using tabulation method.		
Q.17	Using the tabulation method, obtain the simplified expression in product of sums for the Boolean function F(w,x,y,z)=Π(1,3,5,7,13,15).		
Q.18	Simplify the Boolean function F(A,B,C,D,E,F)=Σ(6,9,13,18,19,25,27,29,41,45,57,61) using tabulation method.		
Q.19	**Write short notes on:**		
	(a)	Design of BCD-to-excess-3 code converter	
	(b)	Programmable Logic Array (PLA)	
Q.20	Differentiate between combinational logic circuit and sequential logic circuit. Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.		
Q.21	Design a combinational circuit whose input is a four-bit number and whose output is the 2's complement of the input number.		
Q.22	Design a combinational circuit that converts a decimal digit from the 2,4,2,1 code to the 8,4,-2,-1 code.		
Q.23	Design a combinational circuit that multiplies by 5 an input decimal digit represented in BCD. The output is also in BCD. Show that the output can be obtained from the input lines without using any logic gates.		
Q.24	Design a combinational circuit that converts a four-bit reflected-code number to a four-bit binary number. Implement the circuit with exclusive-OR gates.		

Q.25	Write note on "Binary parallel adder". Also draw logic diagram of a look-ahead carry generator and describe 4-bit full adder with look-ahead carry in detail.	
Q.26	**(a)**	Construct BCD adder using two 4-bit binary parallel adder and logic gates.
	(b)	Explain 4-bit magnitude comparator.
Q.27	Describe decoders using suitable example and design a BCD-to-decimal decoder.	
Q.28	Describe digital multiplexer in detail using suitable example. Obtain an 8×1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines. Use block diagram construction.	
Q.29	**(a)**	Construct a 5 × 32 decoder with four 3 × 8 decoder and a 2 × 4 decoder. Use block diagram construction only.
	(b)	Implement Boolean function $F(A,B,C,D)=\Sigma m(0,1,3,4,8,9,15)$ using 8:1 multiplexer.
Q.30	**(a)**	Design 3-bit binary counter using T flip-flop.
	(b)	Discuss "Digital IC logic families and characteristic of basic gate in each family".
Q.31	Explain race-around condition in relation to the J-K flip-flops using timing relationships. Draw the clocked Master-Slave J-K flip-flop configuration and explain how it removes race-around condition in J-K flip-flops.	
Q.32	Describe triggering of flip-flops and explain operation of an edge triggered D flip-flop.	
Q.33	Write state equations for all flip-flops. Design a sequential circuit with JK flip-flops to satisfy the following state equations: A(t+1)=A'B'CD+A'B'C+ACD+AC'D' B(t+1)=A'C+CD'+ A'BC' C(t+1)=B D(t+1)=D'	
Q.34	Draw the logic diagram of clocked RS Flip-Flop and explain its operation. Design a counter with the following binary sequence: 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use RS flip-flops.	
Q.35	Explain 4-bit synchronous up-down binary counter.	
Q.36	Describe shift registers and explain 4-bit bidirectional shift register with parallel load.	
Q.37	Differentiate between synchronous counter and ripple counter. Explain BCD ripple counter with logic diagram and timing diagram.	
Q.38	**Write Short notes on:**	
	1. Complementary MOS (CMOS) 2. BCD synchronous counter	
Q.39	**Write Short notes on:**	
	1. Emitter-coupled Logic (ECL) 2. Ring counter	
Q.40	**Write Short notes on:**	
	1. Schottky TTL gate 2. 4-bit binary ripple counter	

41	Classify different types of PLDs and briefly explain the architecture of PLDs.
42(a)	Compare PROM, EPROM and EEPROM technologies.
D (b)	Design a PLA which implements the following Boolean functions $F_1=\sum m(0,1,3,4)$ $F_2=\sum m(1,2,3,4,5)$ Realize the same assuming that a 3*4*2 PLA is available.
43	Implement the following Boolean functions using PAL. (i) A=XY+XZ′,B=XY′+YZ′ (ii)A=XY+XZ′,B=XY′+YZ+XZ
44	Realize the following four Boolean functions using PAL. $F_1(W,X,Y,Z) =\sum m(0,1,2,3,7,9,11)$ $F_2(W,X,Y,Z) =\sum m(0,1,2,3,10,12,14)$ $F_3(W,X,Y,Z) =\sum m(0,1,2,3,10,13,15)$ $F_4(W,X,Y,Z) =\sum m(4,5,6,7,9,15)$
45	Build PLA with 5 inputs, 4 outputs and 8 and gates for the following Boolean functions: $F_1= \Sigma(0, 1, 2, 3, 11, 11, 13, 14, 15, 16, 17, 18, 19, 27, 28, 29, 30, 31)$ $F_2= \Sigma(4, 5, 6, 7, 8, 9, 10, 11, 20, 21, 22, 23, 30)$
46	Design a 3-bit binary to Excess-3 code converter using a PROM.
47	Design a combinational circuit using PROM. The circuit accepts a 3 bit number and generates an output binary number equal to square of input number.
48	Design a BCD to excess-3 code converter and implement using suitable PLA.
49	Design a BCD to Gray Code Converter using PAL.
50	Design a 2-bit magnitude comparator using PLA.

	UNIT-V
51(a)	Illustrate the operation of basic flip-flop using NOR gates.
(b)	Explain excitation tables for JK and T flip-flops.
52(a)	Classify different types of Counters.
(b)	Explain the operation of the 4-bit asynchronous counter.
53	Show the operation of a 4-bit shift register using JK flip-flops.
54	Build a 4-bit universal shift register using D flipflops and multiplexers?
55(a)	Construct the D flip-flop with the help of truth table and excitation table.
(b)	Build 4-bit ring counter with circuit diagram, state transition diagram and state table. Draw the corresponding timing diagrams?
56(a)	With suitable logic diagram explain a 4-bit bidirectional shift register?

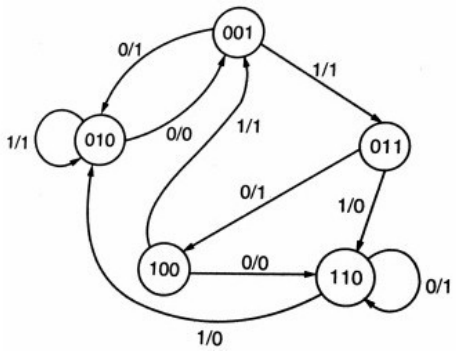
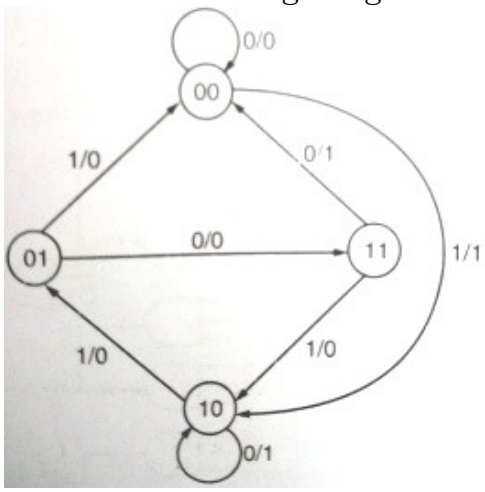
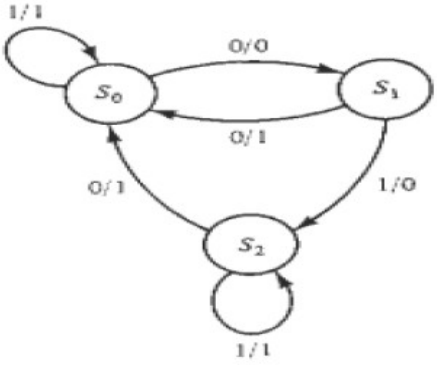
(b)	Develop the design steps of synchronous counters with suitable examples?
57	Design a type-D counter that goes through states 0,2,4,6,0..... The undesired states must always go to a 0 on the next clock pulse.
58	Design a T Flip-Flop from S-R Flip-Flop.
59	Design and implement asynchronous BCD counter using JK filp-flops.
60(a)	Design 5-stage twisted ring counter with circuit diagram, state transition diagram and state table.
(b)	With suitable logic diagrams, distinguish buffer register and controlled buffer register?

61	Explain the following a) State diagram b) State table c) State Assignment rules d) State Reduction Table
62(a)	Draw block diagrams of Moore and Mealy model? Explain.
	(b) Explain capabilities and limitations of finite state machine.
63	Compare Moore and Mealy machine and explain the rules for converting Mealy machine to Moore and vice versa?
64	Convert the following Mealy machine into a corresponding Moore machine.

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

65	Draw the state diagram and circuit excitation table of mod-13 synchronous counter using T flip-flops?
66	Design sequential circuit of Moore model for the following state table?

Present state	Next state		Output
	X=0	X=1	Z
A	A	C	0
B	D	A	0
C	C	A	1
D	B	D	1

67	Draw state diagram in Mealy model for the following state table? | Present state	Next state		Output	
---	---	---	---	---
	X=0	X=1	X=0	X=1
A	A	C	0	1
B	D	A	0	0
C	C	A	1	0
D	B	D	1	0	
68	Design the sequential circuit for the given state diagram shown in figure using JK flip-flops 
69	Design a sequential circuit from the state diagram given below using D-flipflop 
70	A Clocked Sequential Circuits with two inputs x and y and a single output z is defined by the following state diagram. Design the circuit using T-flip-flops. 

71. List the main difference between PLA and PAL.

PLA: Both AND and OR arrays are programmable and Complex, Costlier than PAL.

PAL: AND arrays are programmable OR arrays are fixed, Cheaper and Simpler.

72. List the main difference between PROM and PLA.

In some cases the number of don't care conditions is excessive, it is more economical to

use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however, it does not provide full decoding of the variables and does not generates all the

minterms as in the ROM.

73. List the main difference between ROM and RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can

be read or written into any selected address. RAMs are called as Volatile memories because

RAMs lose stored data when the power is turned OFF.

ROM is a type of memory in which data are stored permanently or semi permanently.

Data can be read from a ROM, but there is no write operation. ROMs are called as Non-Volatile

memories because ROMs doesn't lose stored data when the power is turned OFF.

74. What is Read and Write operation?

The Write operation stores data into a specified address into the memory and the Read

operation takes data out of a specified address in the memory.

75. How many words can a12x8 memory can store?

A 12x8 memory can store 4096 words of eight bits each.

76. Define ROM and RAM.

RAM is Random Access Memory. It is a random access read/write memory. The data can

be read or written into any selected address. RAMs are called as Volatile memories because

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memories because ROMs doesn't lose stored data when the power is turned OFF.

77. Define Static RAM and Dynamic RAM.

Static RAM use flips flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

78. Define PLA.

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.

79. Compare Hamming code and Parity code

A parity bit is a bit appended to a data of binary bits to ensure that the total number of 1's in the data is even or odd. The simple parity code cannot correct errors, but it can detect error.

Even parity bit:

In the case of even parity, for a given set of bits, the numbers of 1's are counted. If that count is odd, the parity bit value is set to 1, making the total count of occurrences of 1's an even number. If the total number of 1's in a given set of bits is already even, the parity bit's value is 0.

Odd parity bit:

In the case of odd parity, for a given set of bits, the numbers of 1's are counted. If that count is even, the parity bit value is set to 1, making the total count of occurrences of 1's an odd number. If the total number of 1's in a given set of bits is already odd, the parity bit's value is 0.

Hamming code is a set of error-correction codes that can be used to detect and correct the errors that can occur when the data is moved or stored from the sender to the receiver.

80. What is PLD?

A programmable logic device is an electronic component used to build reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an undefined function at the time of manufacture.

81. Summarize about FPGA.

• A field-programmable gate array (FPGA) is a VLSI circuit that can be programmed at the

user's location.

• A typical FPGA consists of an array of millions of logic blocks, surrounded by programmable input and output blocks and connected together via programmable interconnections.

• A typical FPGA logic block consists of lookup tables, multiplexers, gates, and flip-flops. A lookup table is a truth table stored in an SRAM and provides the combinational circuit functions for the logic block.

82. Define Asynchronous sequential circuit.

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

The circuit is considered to be asynchronous if it does not employ a periodic clock signal to synchronize its internal changes of state. Therefore the state changes occur in direct response to signal changes on primary (data) input lines, and different memory elements can change state at different times.

83. What are the steps for the design of asynchronous sequential circuit?

▪ Construction of a primitive flow table from the problem statement.

▪ Primitive flow table is reduced by eliminating redundant states using the state reduction

▪ State assignment is made

o The primitive flow table is realized using appropriate logic elements.

84. What are races?

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit