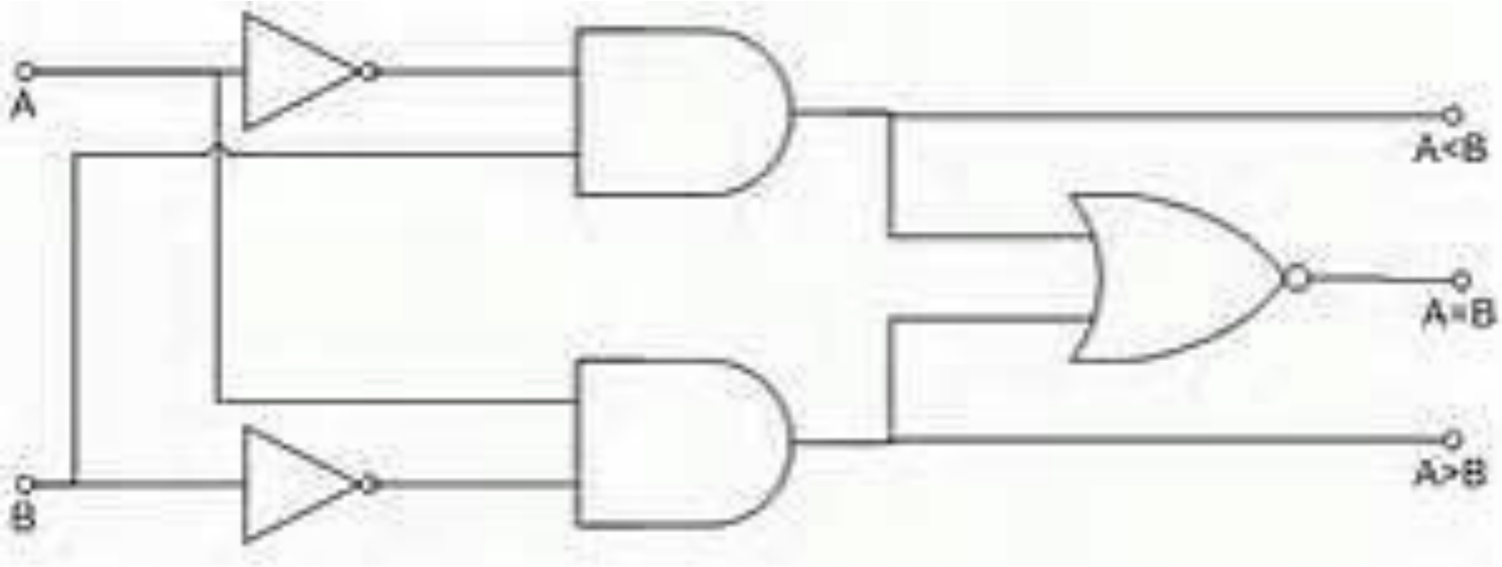
Exp No. 2 Magnitude Comparator

Two 1-bit magnitude comparator

A	B	E(A=B)	G(A>B)	L(A<B)
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0
		$\bar{A}\bar{B} + AB$	$A\bar{B}$	$\bar{A}B$



1-bit magnitude comparator

2-bit comparator

- The block diagram of a two-bit comparator which has four inputs and three outputs is shown below.
- The first number A is designated as A = A1A0 and the second number is designated as B = B1B0.
- This comparator produces three outputs as G (G = 1 if A>B), E (E = 1, if A = B) and L (L = 1 if A<B).

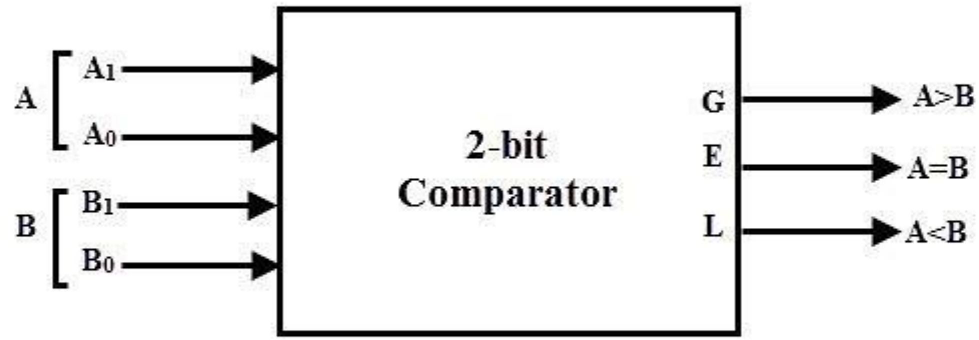


Table 1. Truth Table of 2-Bit Magnitude Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

- Using k-map:
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$$A>B: G = A0\,\overline{B1}\;\overline{B0} + A1\,\overline{B1} + A1\,A0\,\overline{B0}$$

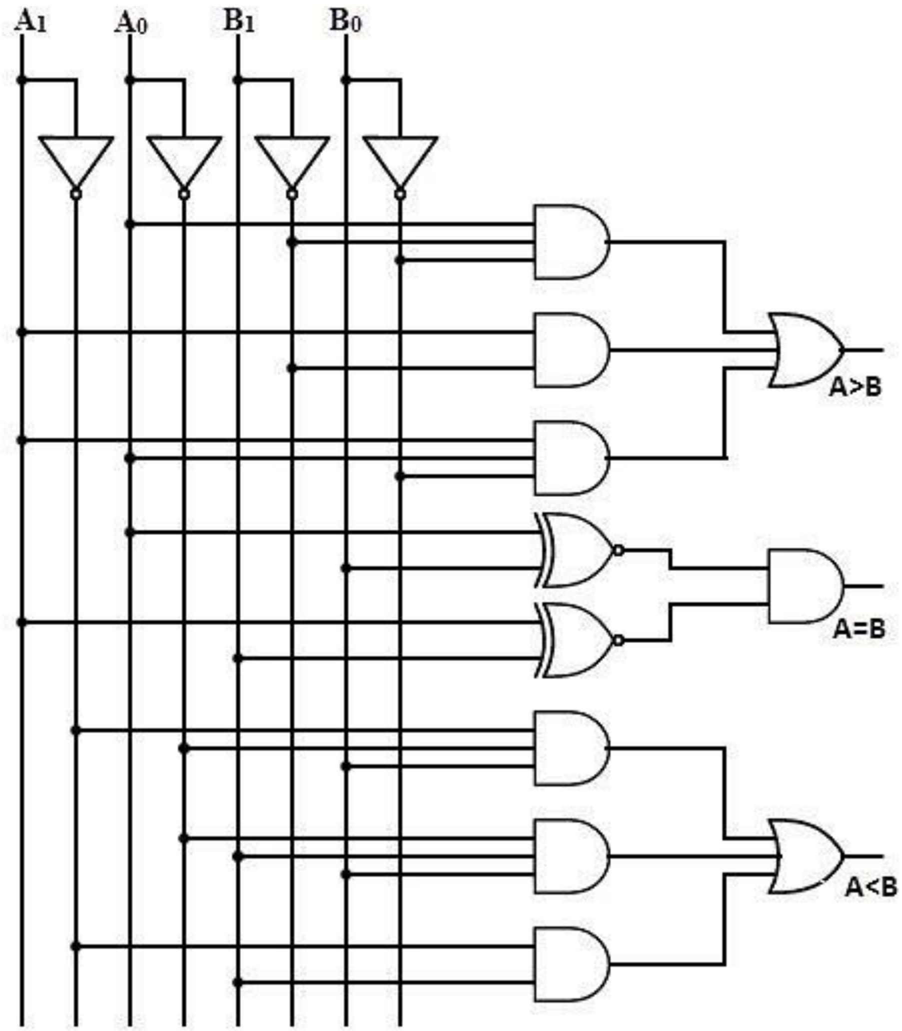
$$A=B: E = \overline{A1}\;\overline{A0}\;\overline{B1}\;\overline{B0} + \overline{A1}\,A0\;\overline{B1}\,B0 + A1\,A0\,B1\,B0 + A1\,\overline{A0}\,B1\,\overline{B0}$$

$$= \overline{A1}\;\overline{B1}\,(\overline{A0}\;\overline{B0} + A0\,B0) + A1\,B1\,(A0\,B0 + \overline{A0}\;\overline{B0})$$

$$= (A0\,B0 + \overline{A0}\;\overline{B0})\,(A1\,B1 + \overline{A1}\;\overline{B1})$$

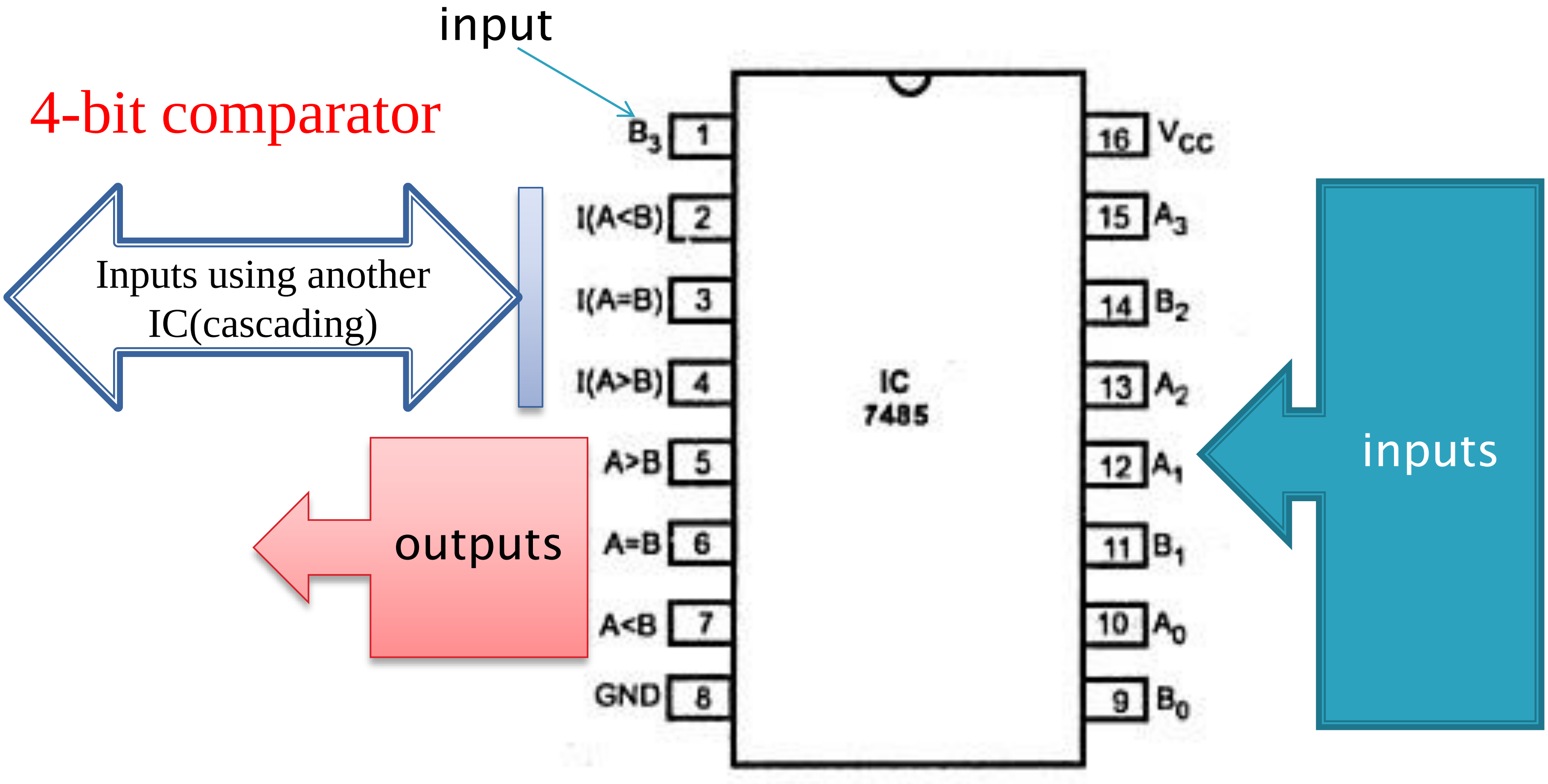
$$= (A0 \text{ Ex-NOR } B0)\,(A1 \text{ Ex-NOR } B1)$$

$$A<B: L = \overline{A1}\;B1 + \overline{A0}\,B1\,B0 + \overline{A1}\;\overline{A0}\,B0$$



Two bit comparator logic diagram

4-bit comparator



(a) Pin diagram (IC 7485)

- It can be used to compare two four-bit words.
- The two 4-bit numbers are A = A3 A2 A1 A0 and B3 B2 B1 B0 where A3 and B3 are the most significant bits.

8-bit comparator

- An 8-bit comparator compares the two 8-bit numbers by **cascading** of two 4-bit comparators.
- The circuit connection of this comparator is shown below in which the lower order comparator A<B, A=B and A>B outputs are connected to the respective cascade inputs of the higher order comparator.