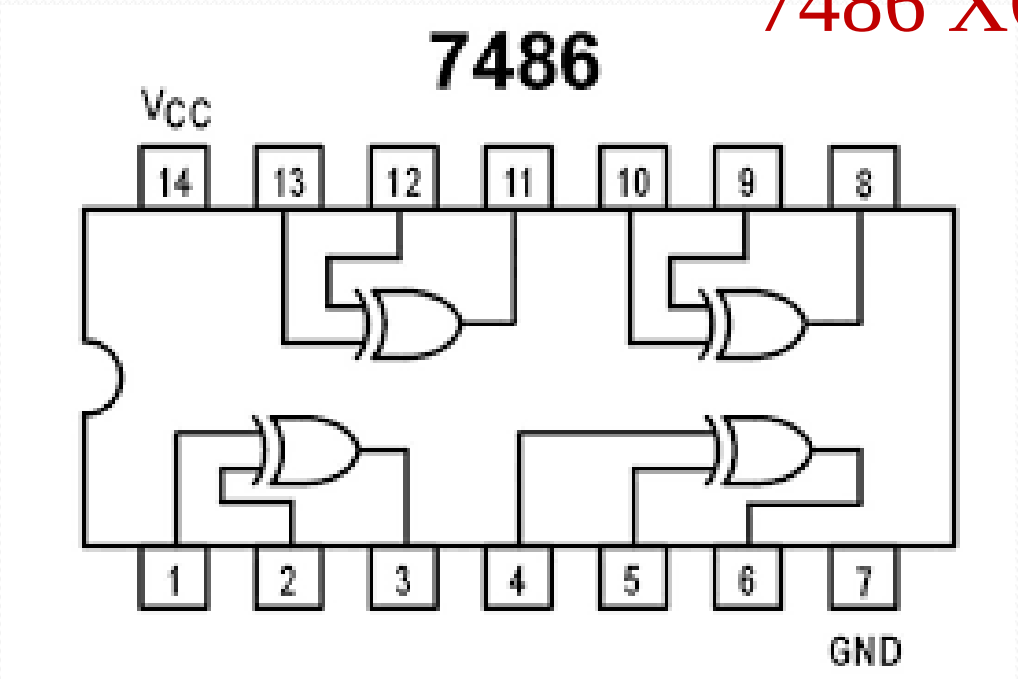
Exp. No. 3 Parity generator-checker and controlled inverter

- **One important application of the use of an Exclusive-OR gate is to generate parity.**
- Parity is used to detect errors in transmitted data caused by noise or other disturbances.
- A parity bit is an extra bit that is added to a data word and can be either odd or even parity.
- In an even parity system, the sum of all the bits (including the parity bit) is an even number
- In an odd parity system the sum of all the bits must be an odd number.

- The circuit that creates the parity bit at the transmitter is called the parity generator.
- The circuit that determines if the received data is correct is the parity checker.
- **Parity is good for detecting a single bit error only.**
- The parity generator and the parity checker can both be built using Exclusive-OR gates.
- *In **even parity** bit scheme, the parity bit is '**0**' if there are **even number of 1s** in the data stream and the parity bit is '**1**' if there are **odd number of 1s** in the data stream.*

- *In **odd parity** bit scheme, the parity bit is '**1**' if there are **even number of 1s** in the data stream and the parity bit is '**0**' if there are **odd number of 1s** in the data stream.*

7486 XOR



Even Parity Generator

- The total number of 1s must be **even**, to generate the even parity bit P.

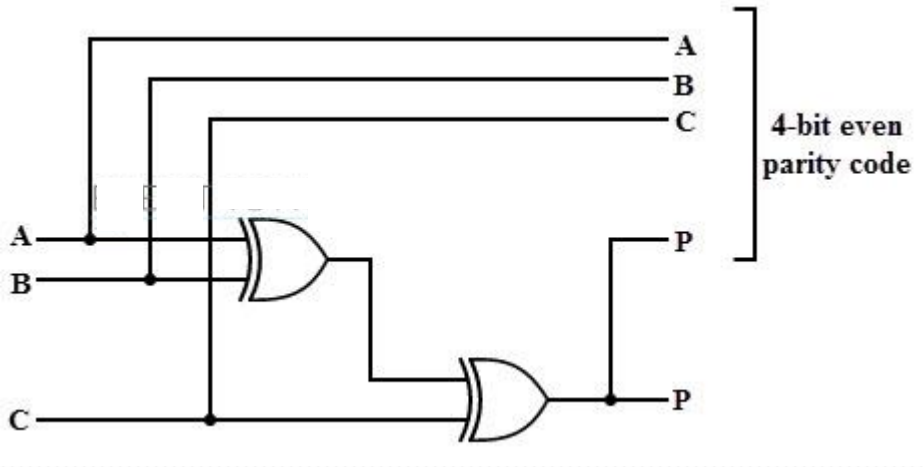
3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$P = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,\bar{C} + A\,B\,C$$

$$= \bar{A}\,(\bar{B}\,C + B\,\bar{C}) + A\,(\bar{B}\,\bar{C} + B\,C)$$

$$= \bar{A}\,(B \oplus C) + A\,(\overline{B \oplus C})$$

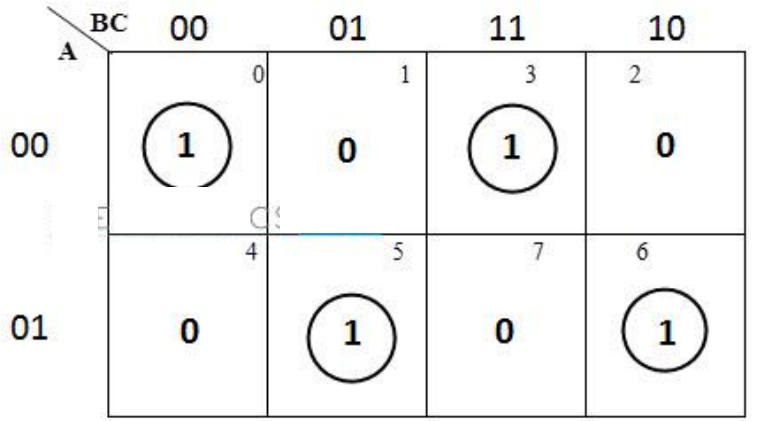
$$P = A \oplus B \oplus C$$



Odd Parity Generator

- The total number of 1s must be **odd**, to generate the even parity bit P.

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



H.W: find the expression of odd parity generator from k-map and plot its logic circuit

Even Parity Checker

The below table shows the truth table for the even parity checker in which **parity error check (PEC) = 1 if the error occurs, i.e., the four bits received have odd number of 1s** and *PEC = 0 if no error occurs, i.e., if the 4-bit message has even number of 1s.*

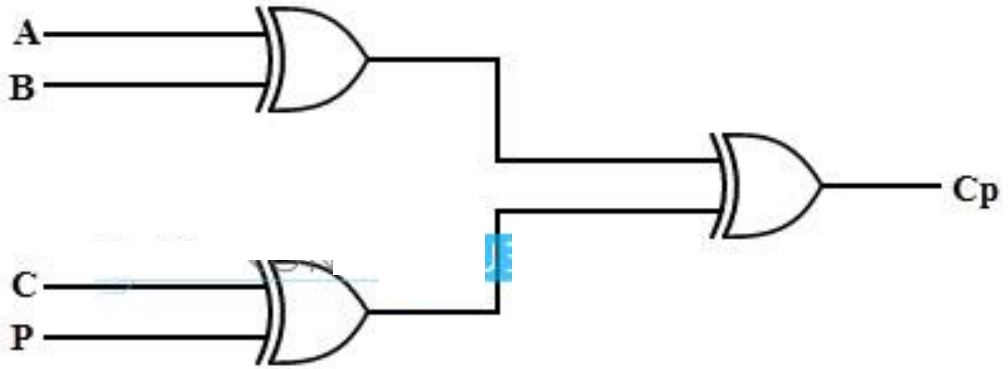
4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

$$PEC = \bar{A}\ \bar{B}\ (\bar{C}\,D + C\,\bar{D}) + \bar{A}\,B\,(\bar{C}\,\bar{D} + C\,D) + A\,B\,(\bar{C}\,D + C\,\bar{D}) + A\,\bar{B}\,(\bar{C}\,\bar{D} + C\,D)$$

$$= \bar{A}\ \bar{B}\,(C \oplus D) + \bar{A}\,B\,(\overline{C \oplus D}) + A\,B\,(C \oplus D) + A\,\bar{B}\,(\overline{C \oplus D})$$

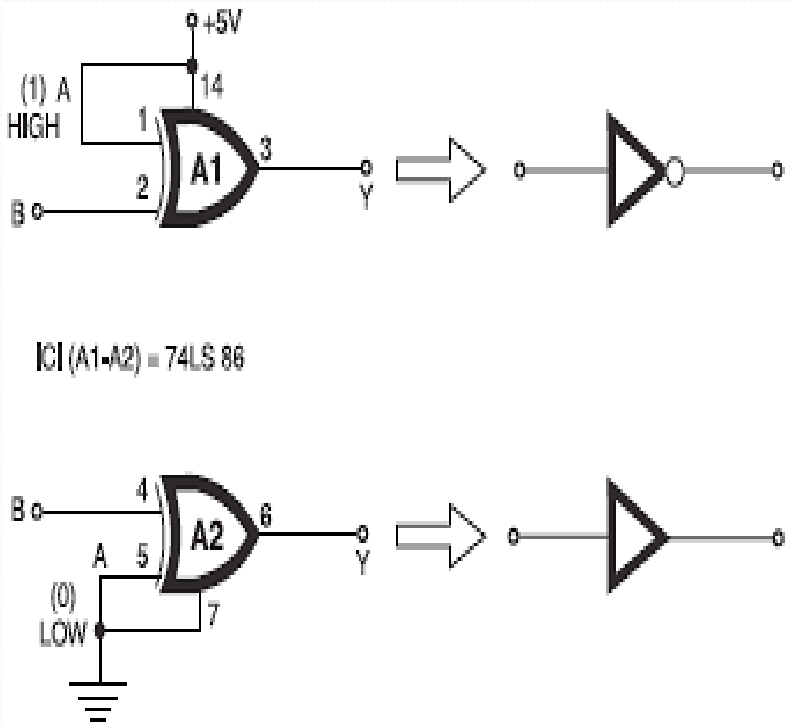
$$= (\bar{A}\ \bar{B} + A\,B)\,(C \oplus D) + (\bar{A}\,B + A\,\bar{B})\,(\overline{C \oplus D})$$

$$= (A \oplus B) \oplus (C \oplus D)$$



Controlled inverter

It can be seen from the figure and the accompanying truth table that **XOR gate works as NOT (inverter) gate when its one input is held high**, *and as a buffer when the* ***same input*** *is pulled low.*



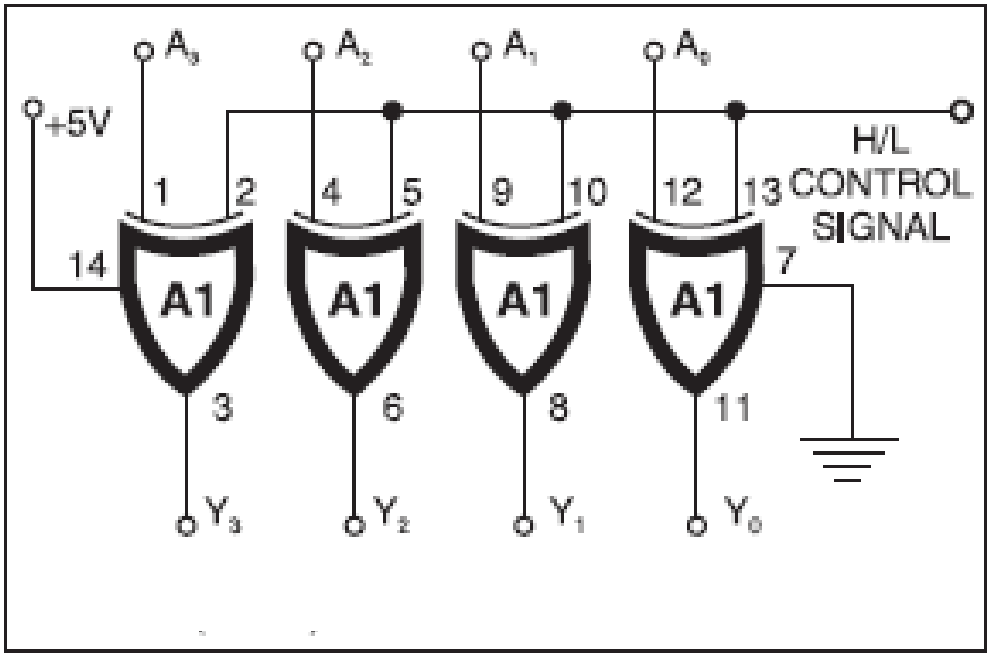
TRUTH TABLE I
XOR Gate

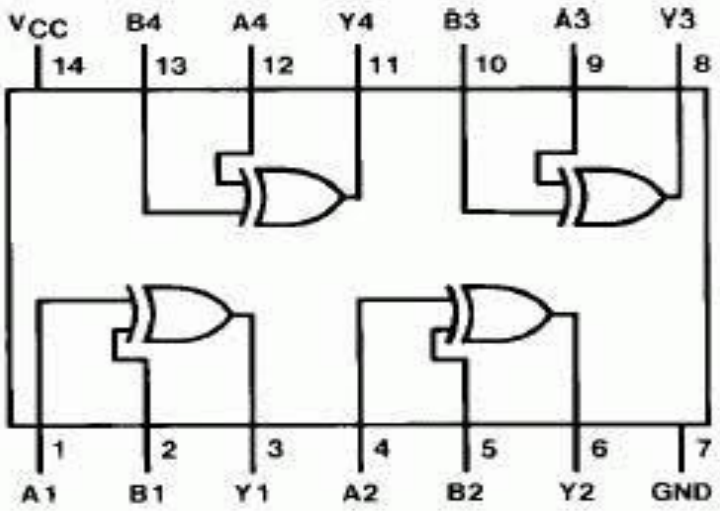
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A=1, then B'=Y and B=Y'

B=1, then A=Y' and A'=Y

XOR gate as controlled inverter





7486 XOR