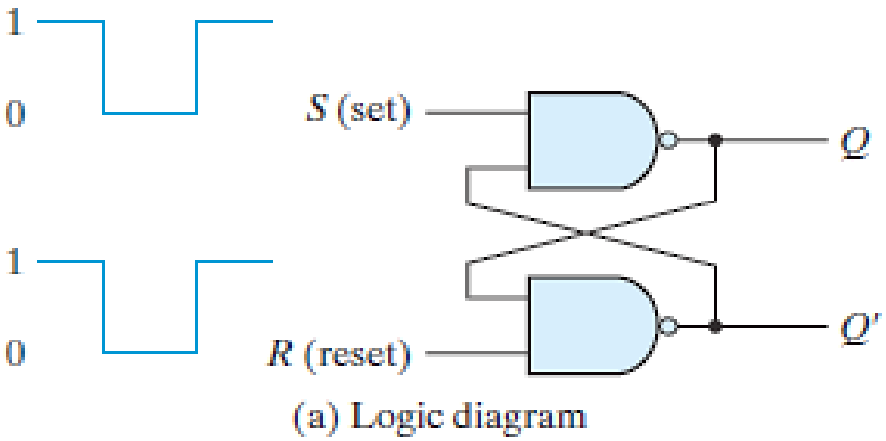
Exp. No.6 Flip-Flops

By: Assistant Professor Maha George Zia

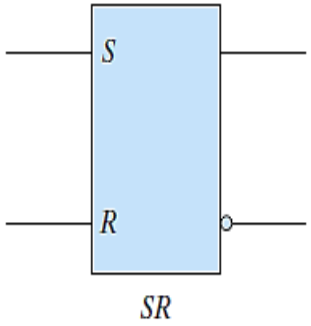
SR- Latch (without clock)

- Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches ; those controlled by a clock transition are flip-flops .
- Latches are said to be level sensitive devices; flip-flops are edge-sensitive devices.



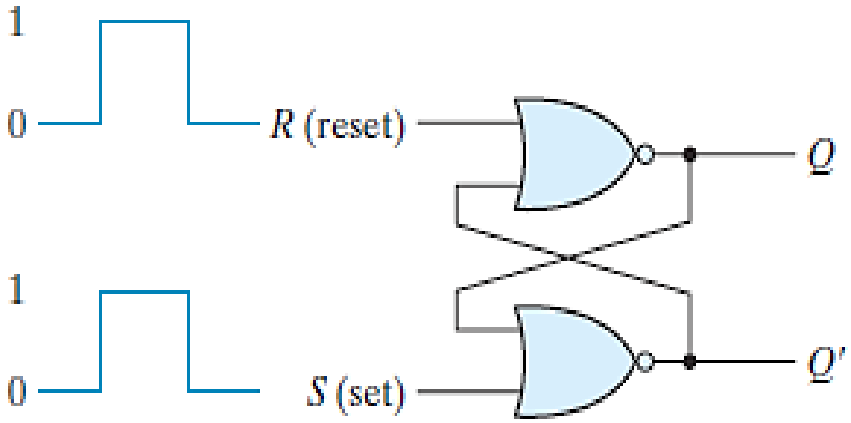
(a) Logic diagram

(a) SR latch with NAND gates



(b) SR Latch block diagram

- **Note: Each flip flop is a binary cell capable of storing one bit of information. For example to store 4-bits we need 4 flip-flops.**



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

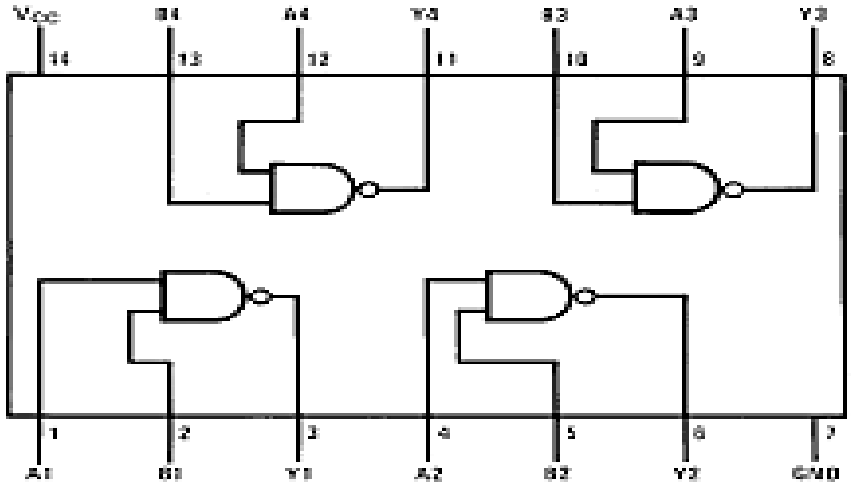
SR latch with NOR gates

(a) Response to positive level

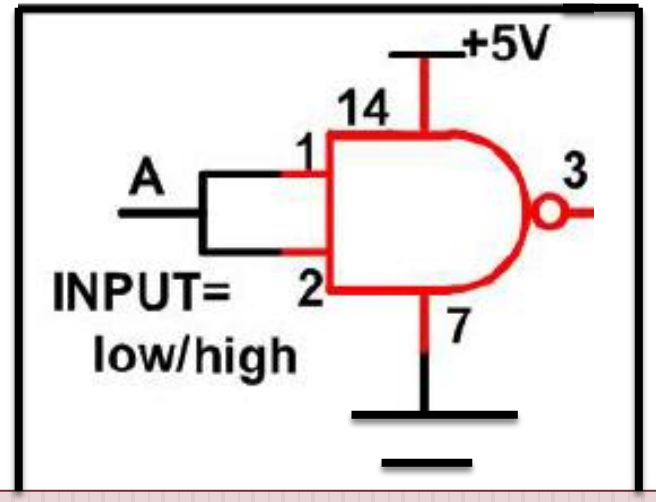
(b) Positive-edge response

(c) Negative-edge response

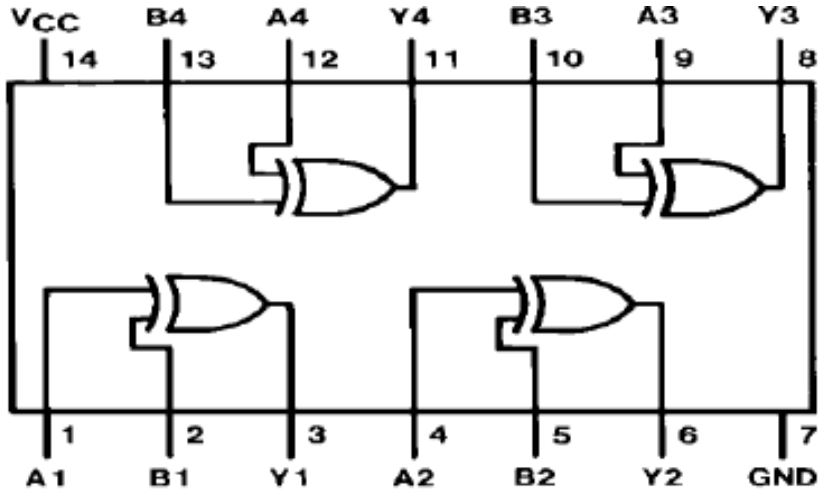
(a) response in latch and (b,c) clock applied to flip-flop



Pin diagram of 7400N NAND



NAND gate connected as NOT gate



Pin diagram of 7486 XOR

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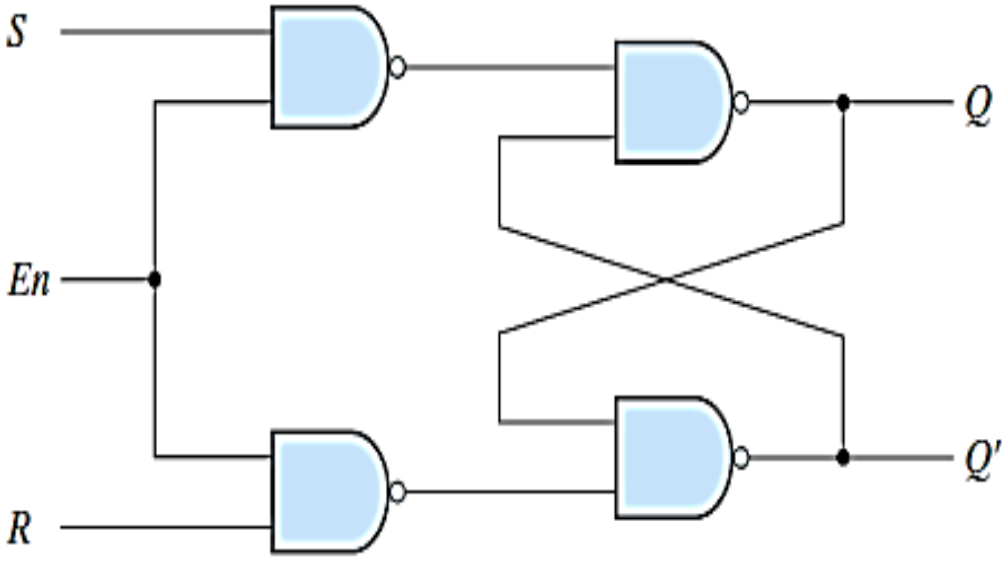
SR Flip-Flop

- flip-flops are edge-sensitive devices and controlled by clock(clk, cp, En, Enable)



(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

SR Flip - Flop

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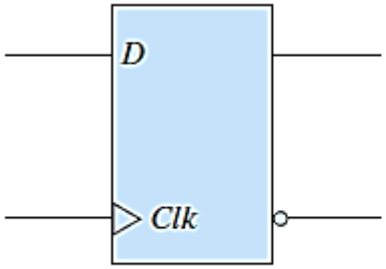
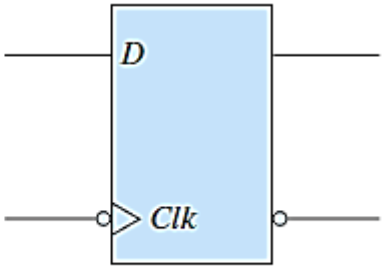
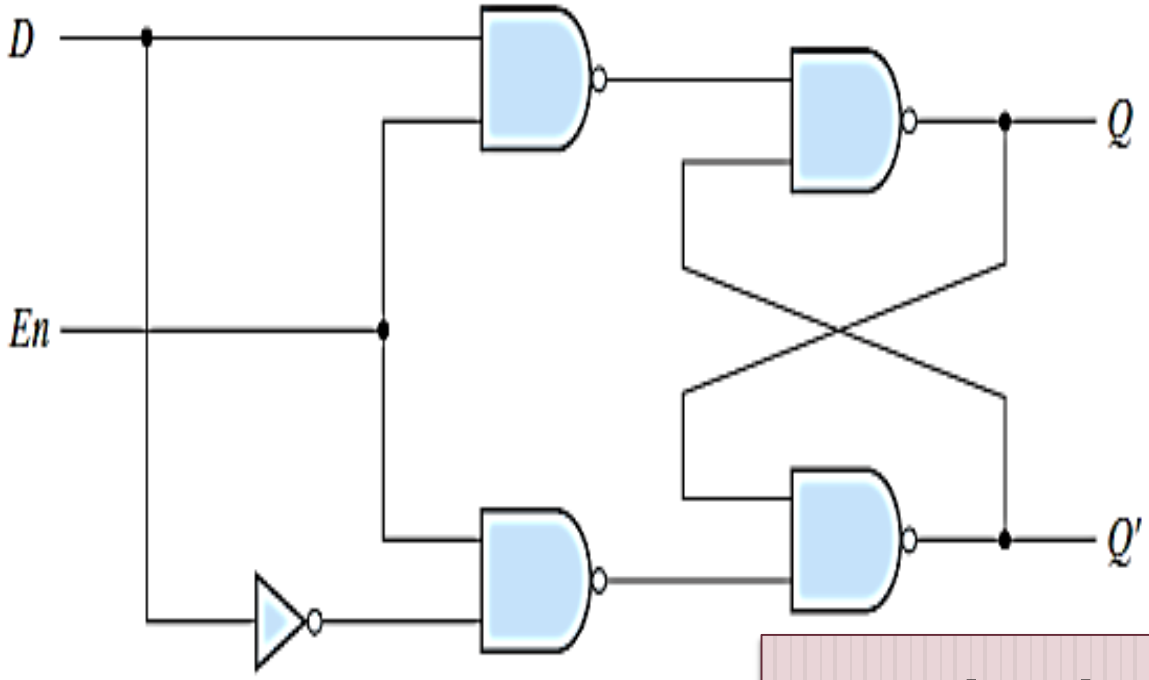
D Flip-Flop



(a) Positive-edge



(a) Negative-edge



(a) Logic diagram

En	D	Next state of Q
0	X	No change
1	0	Q = 0; reset state
1	1	Q = 1; set state

(b) Function table

D Flip-Flop

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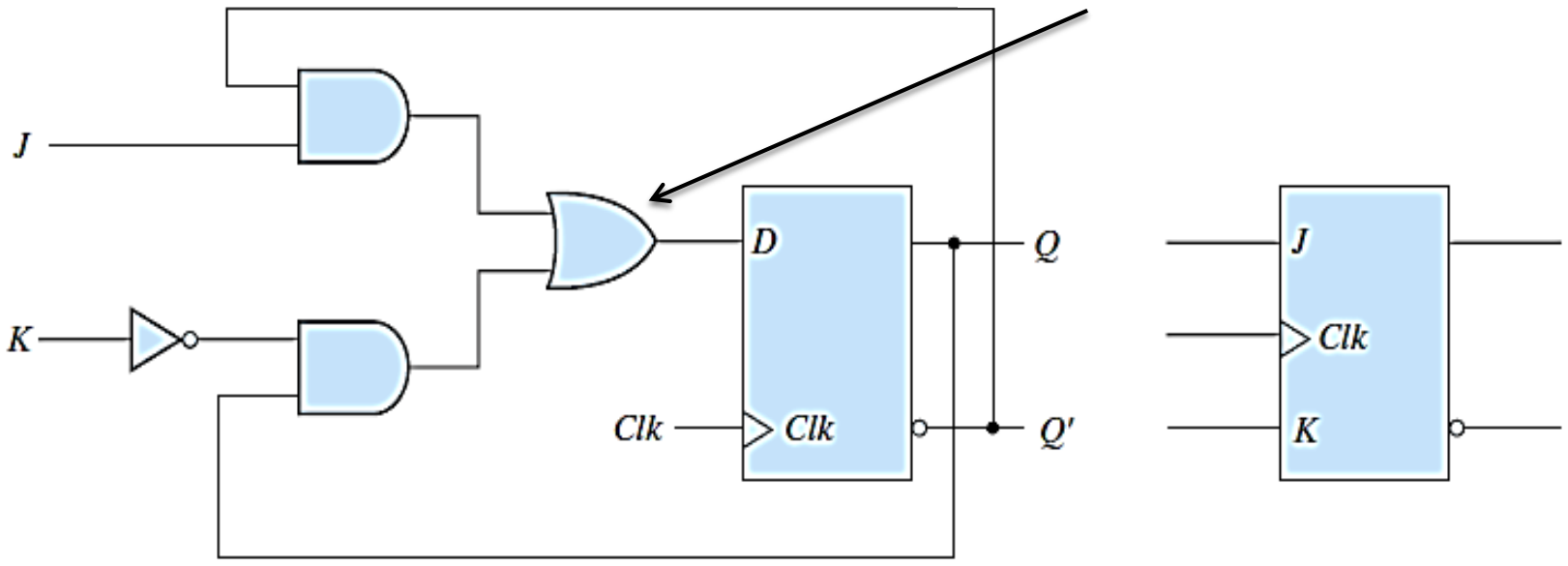
JK Flip-Flop

$$D = JQ' + K'Q$$



(a) Circuit diagram (b) Graphic symbol

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

JK Flip-Flop Characteristic Tables

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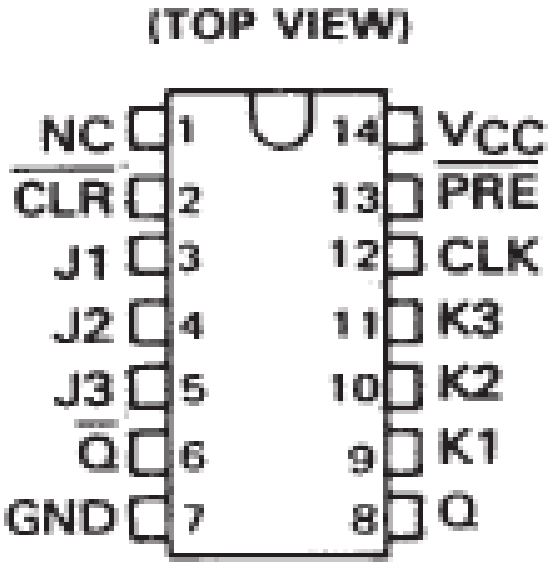
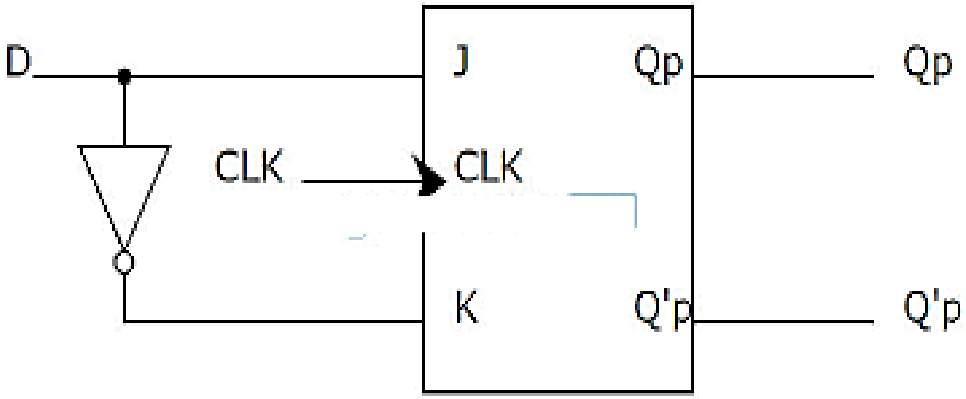
7472 IC (JK FF)



$$D = JQ' + K'Q$$

If K = D' , and J= D then D = DQ' + DQ = D and the JK flip flop is connected as D Flip flop.



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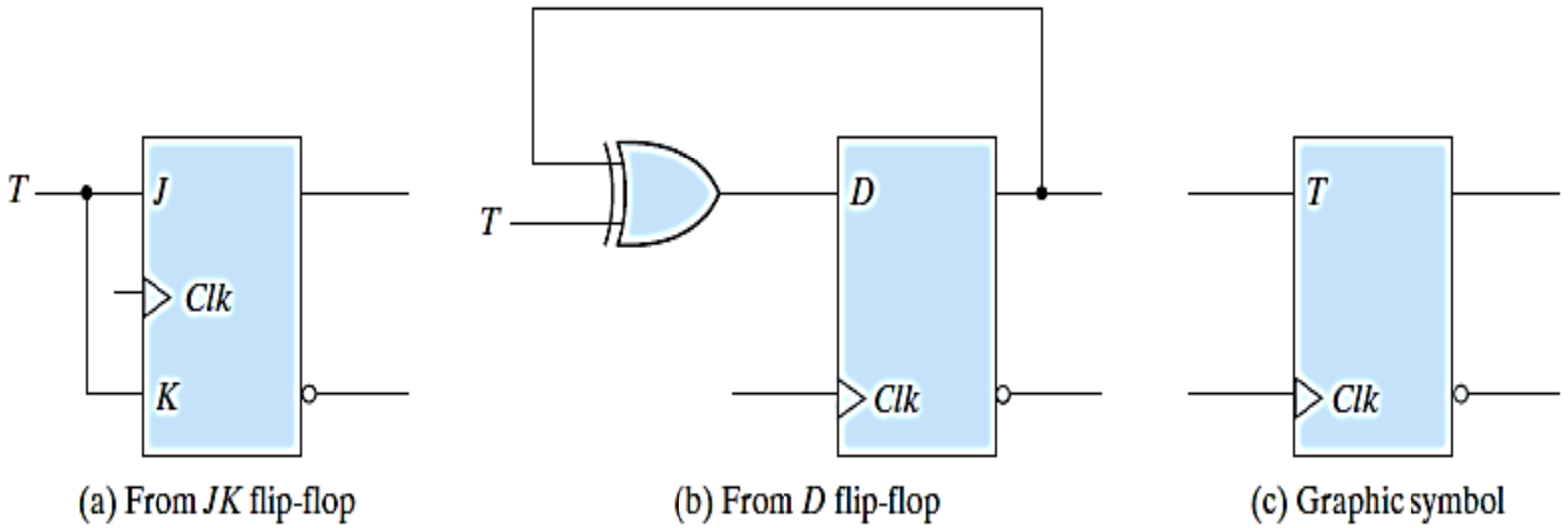
T Flip Flop (Toggle)



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

If T = 0 (J = K = 0), a clock edge does not change the output. When T = 1 (J = K = 1), a clock edge complements the output

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

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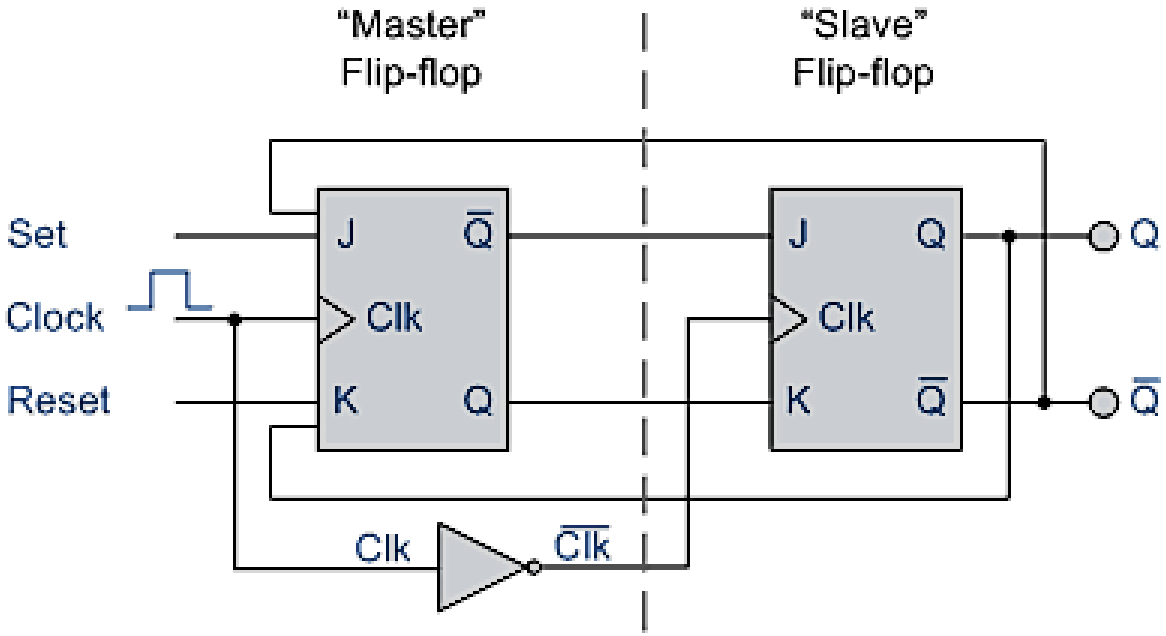
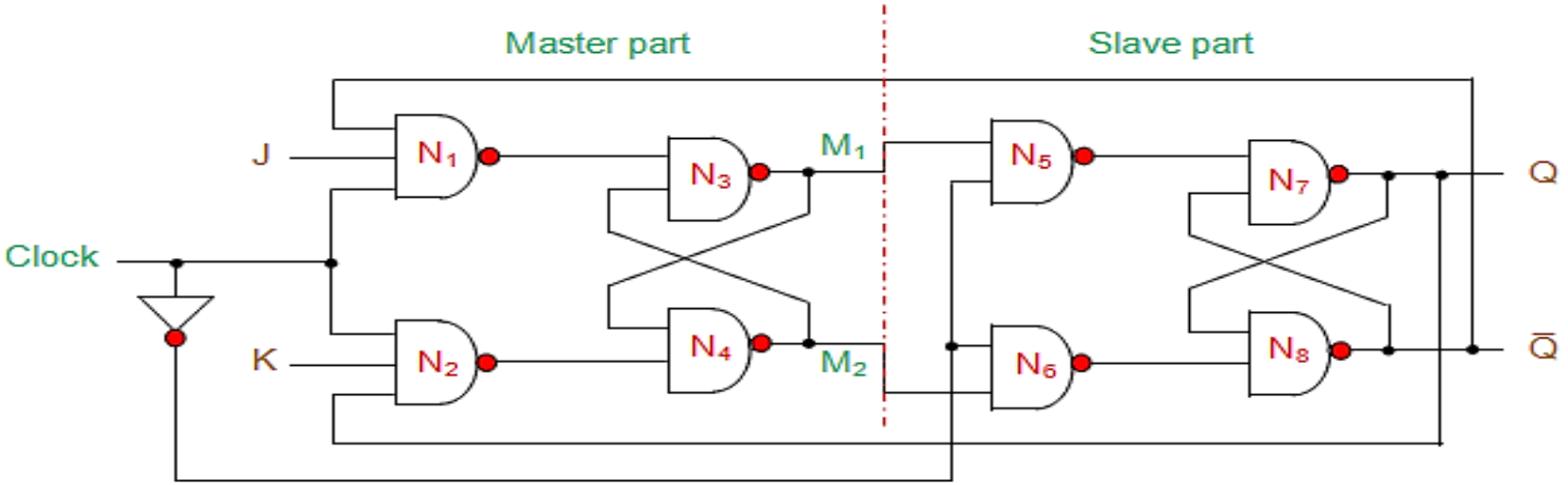
Master-Slave JK Flip Flop

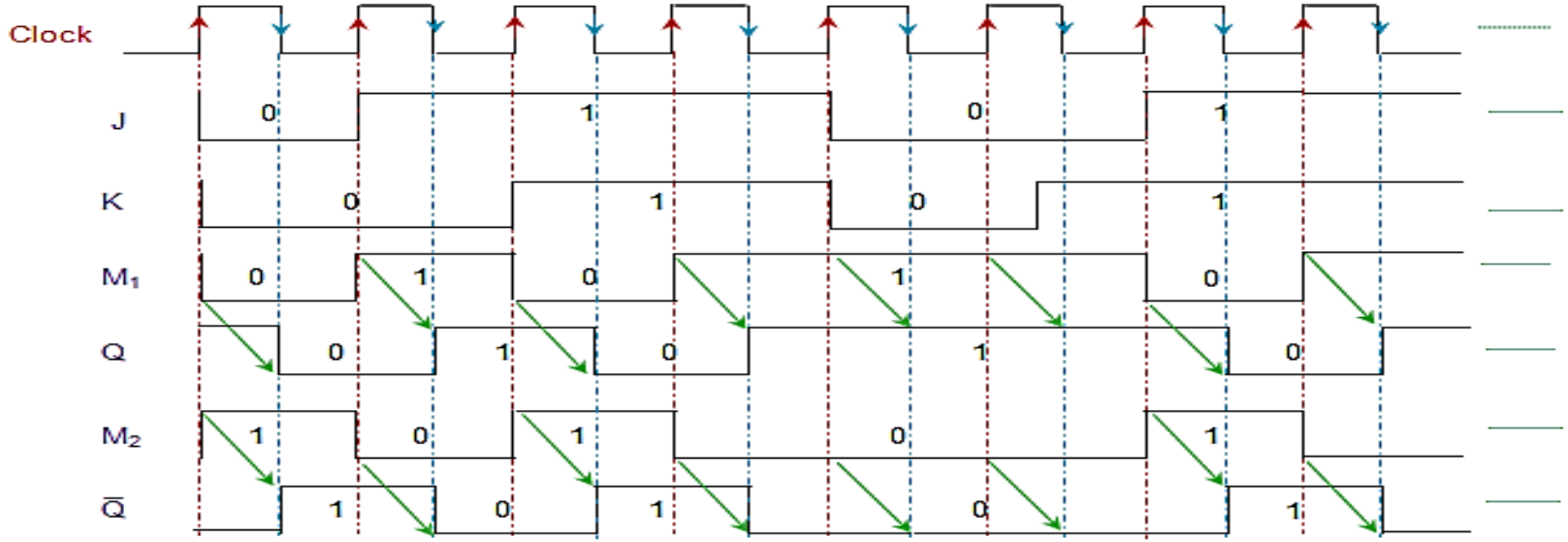
Master-slave flip flop is designed using two separate flip flops. Out of these, one acts as the master and the other as a slave.



- From the above figure you can see that both the J-K flip flops are presented in a series connection. The output of the master J-K flip flop is fed to the input of the slave J-K flip flop. The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop. The clock pulse [Clk] is given to the master J-K flip flop and it is sent through a NOT Gate and thus inverted before passing it to the slave J-K flip flop.
- Here the master flip-flop is triggered by the external clock pulse train while the slave is activated at its inversion i.e. if the master is positive edge-triggered, then the slave is negative-edge triggered and vice-versa.



Master-Slave JK flip-flop realized using NAND gates and an inverter



Timing diagram for master-slave JK flip-flop