Exp. No. 7 Counters

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Registers and counters

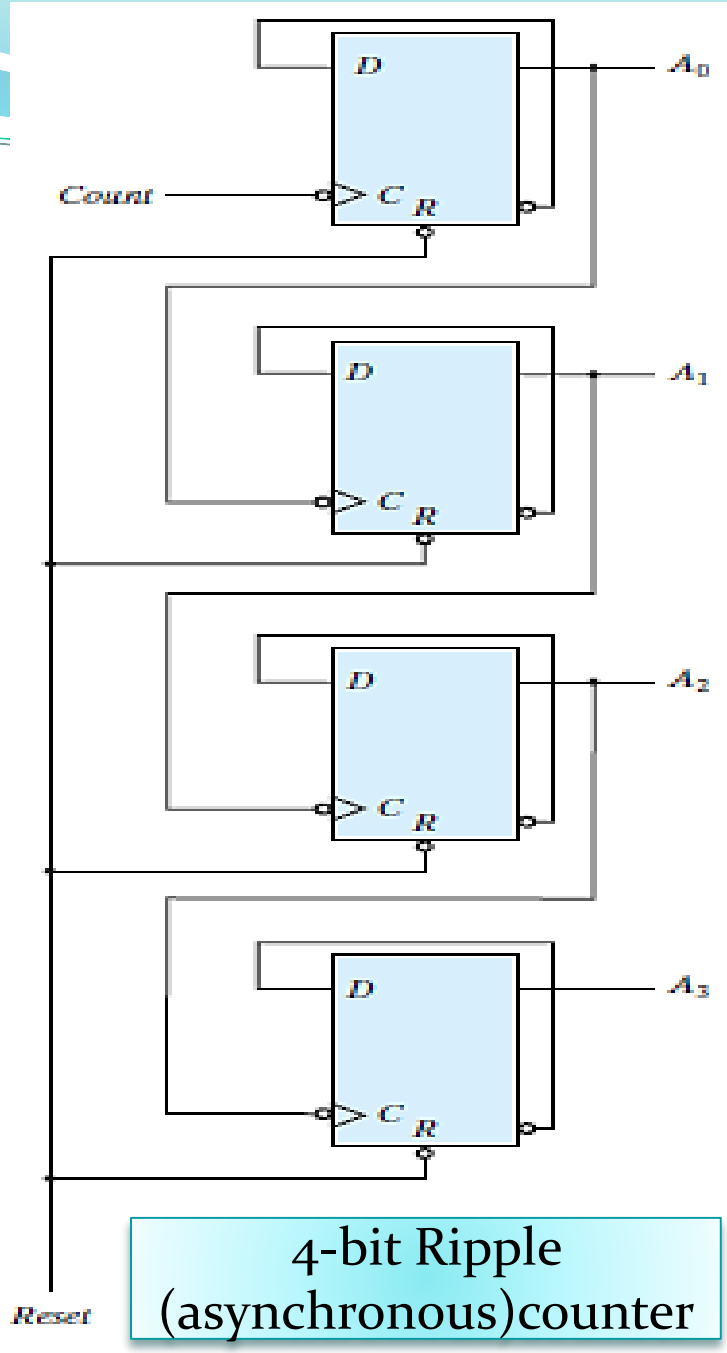
- A *register* is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information.
- An *n* -bit register consists of a group of *n* flip-flops capable of storing *n* bits of binary information
- A *counter* is essentially a register that goes through a predetermined sequence of binary states(MOD)
- **Number of states = 2 (number of flip flops)**
- **An *n* -bit binary counter (mod n) consists of *n* flip-flops and can count in binary from 0 through 2^n - 1.**

Counter Types

Ripple, serial or asynchronous counter

Parallel, synchronous counter

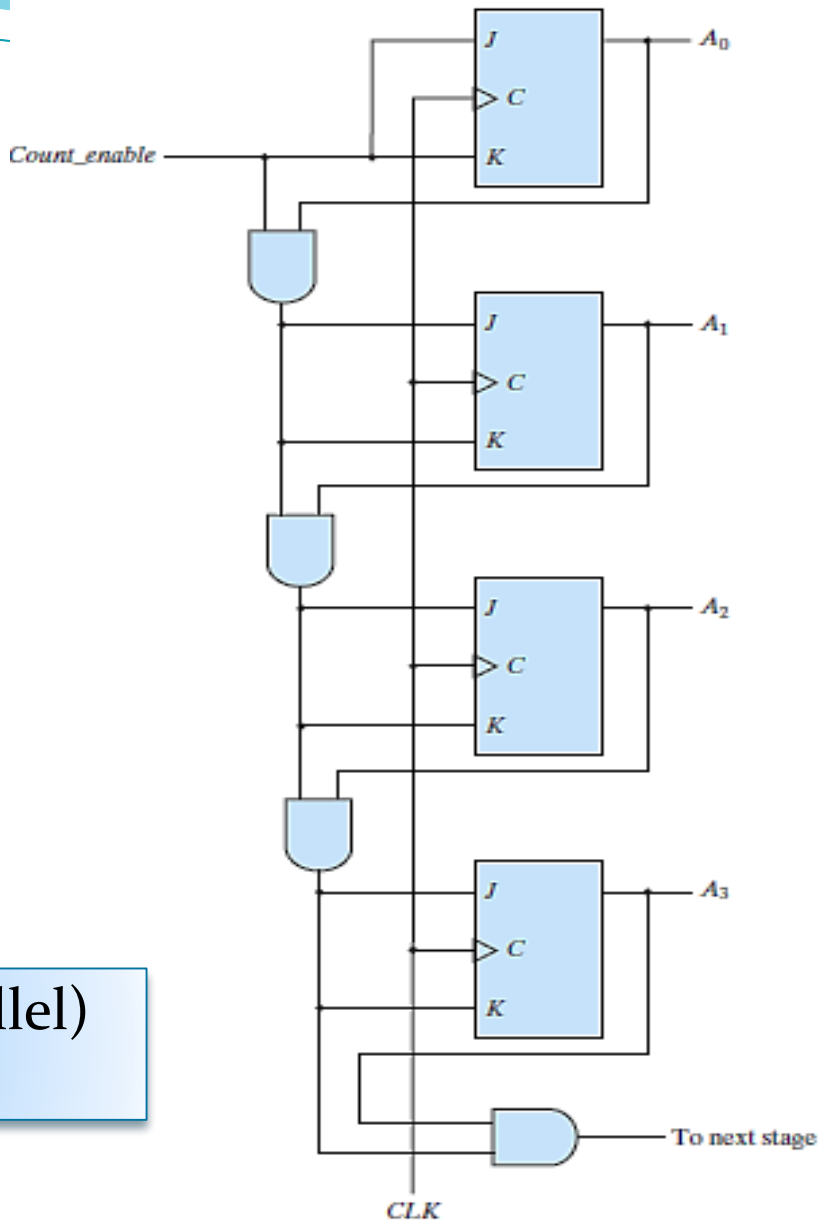
In a ripple (asynchronous) counter, a flip-flop output transition serves as a source for triggering other flip-flops.



4-bit Ripple (asynchronous)counter

In a synchronous (parallel) counter, the *Clock* inputs of all flip-flops receive the common clock.

The synchronous counter can be triggered with either the positive or the negative clock edge

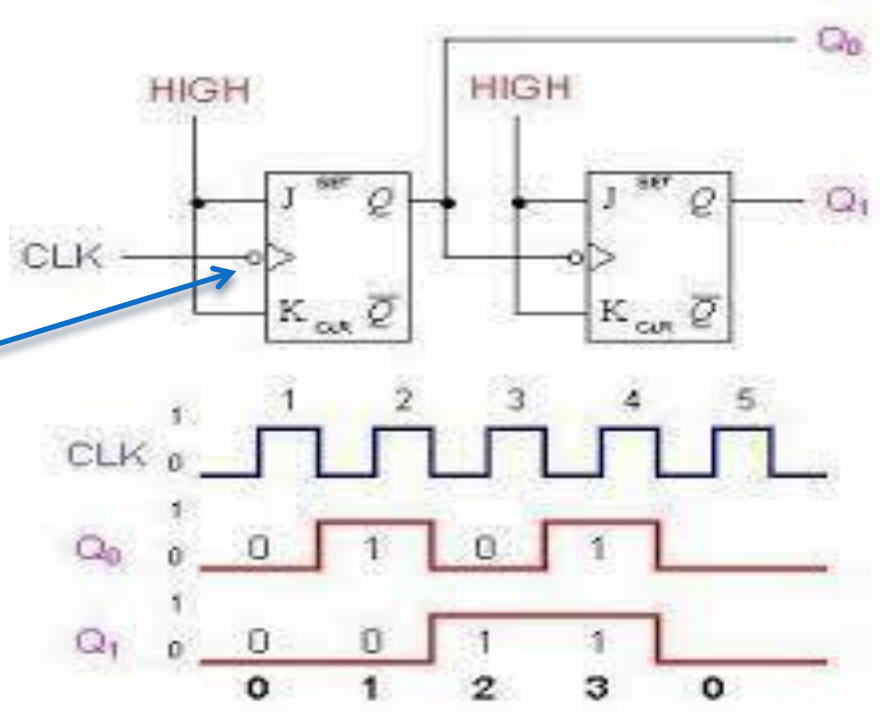


4-bit synchronous(parallel) counter

Asynchronous Up counter and Asynchronous Down counter

- A **four-bit binary ripple counter**, can count in up counter from 0000 to 1111 and can count in down counter from 1111 to 0000 because **number of states= $2^4 = 16$**
- The polarity of the clock is important in asynchronous (ripple) counter.
- A binary countdown counter is a binary ripple counter provided that all flip-flops trigger on the positive edge of the clock.
- A binary **count-up** counter is a binary ripple counter provided that all flip-flops trigger on the **negative edge** of the clock.

Negative clock polarity

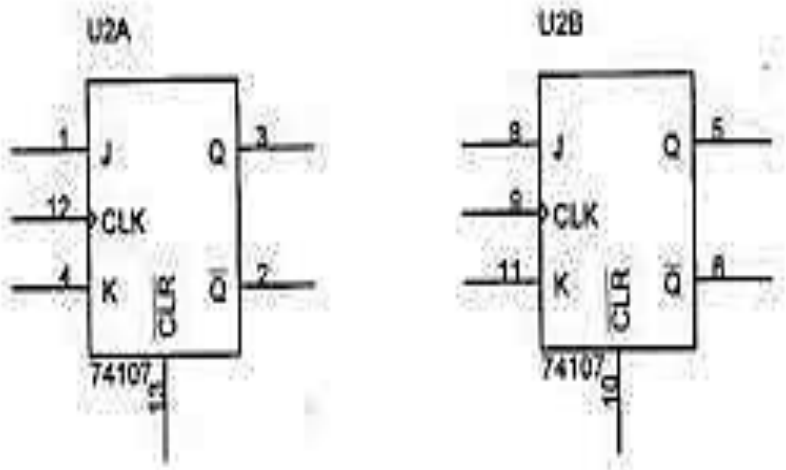


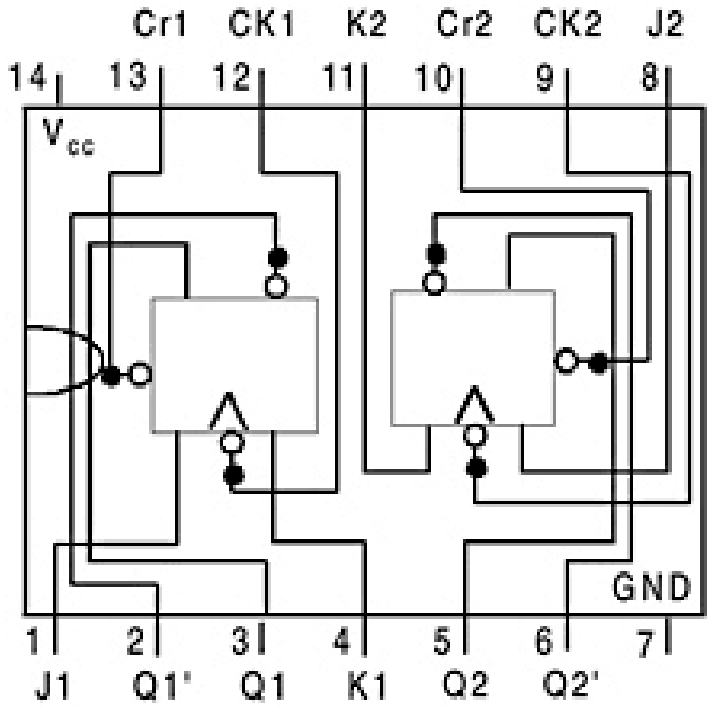
We have 2 flip flops, then number of states= 2^2 = 4, which are 0,1,2,3 or 00, 01,10, 11

2-bit ripple up counter and its timing diagram

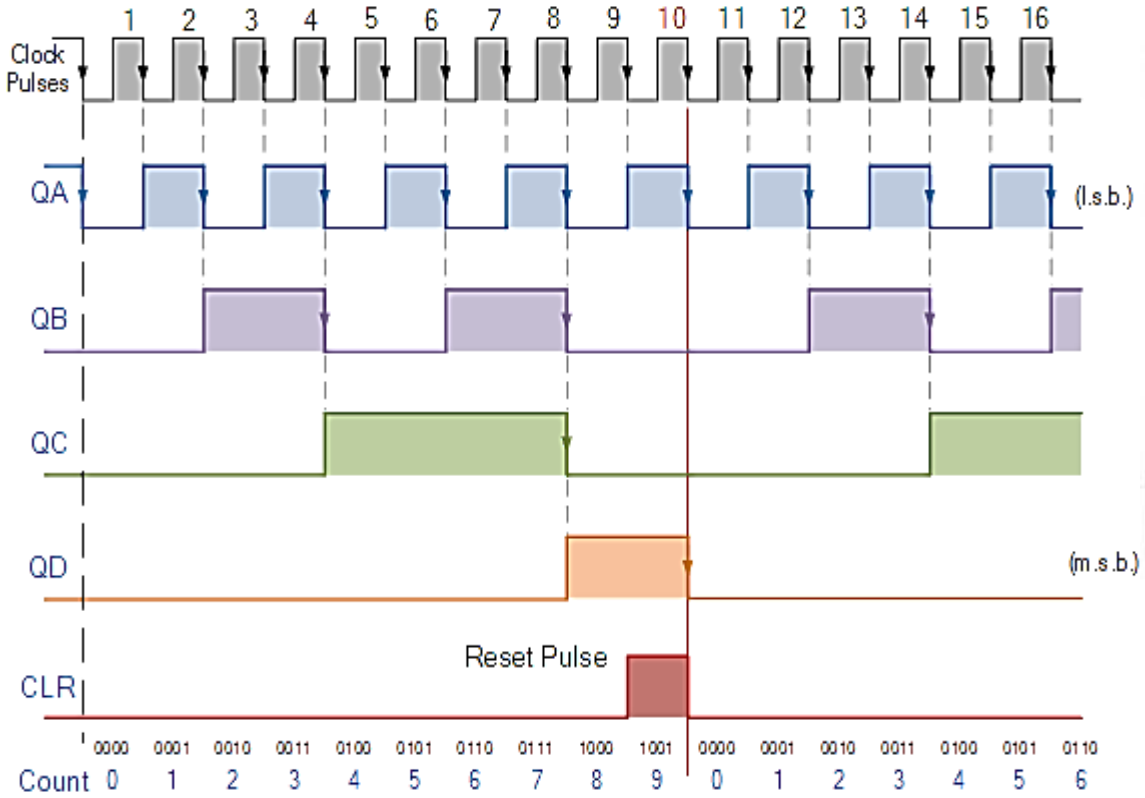
H.W plot 2-bit ripple down counter and plot its timing diagram

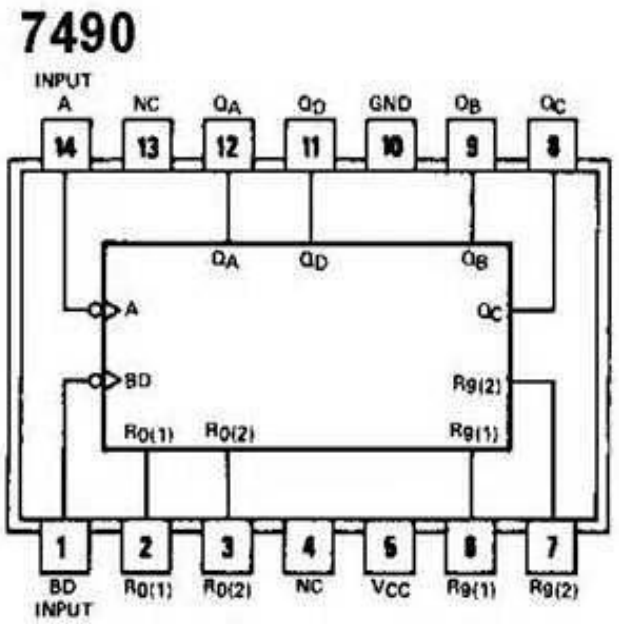
74107 Dual J-K flip-flop with reset; negative-edge trigger





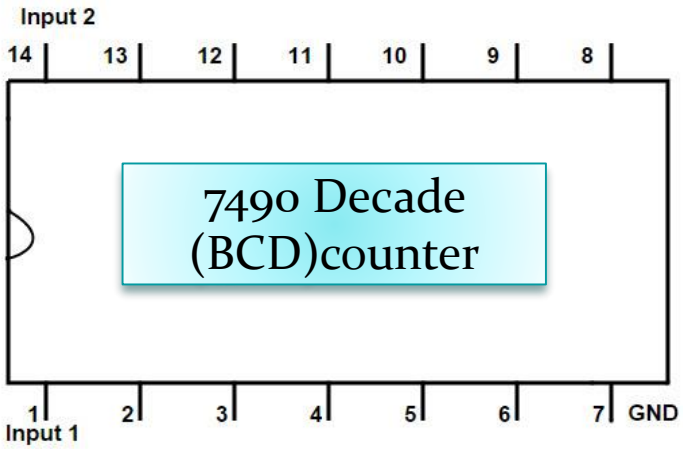
Decade (BCD) Counter





it counts from 0 to 9

Pin No	Function	Name
1	Clock input 2	Input2
2	Reset1	R1
3	Reset2	R2
4	Not connected	NC
5	Supply voltage; 5V (4.75V – 5.25V)	Vcc
6	Reset3	R3
7	Reset4	R4
8	Output 3, BCD Output bit 2	Q_C
9	Output 2, BCD Output bit 1	Q_B
10	Ground (0V)	Ground
11	Output 4, BCD Output bit 3	Q_D
12	Output 1, BCD Output bit 0	Q_A
13	Not connected	NC
14	Clock input 1	Input1



- To count in decimal from 0 to 99, we need a two-decade counter. To count from 0 to 99, we need a three-decade counter.
- **Multiple decade counters can be constructed by connecting BCD counters in cascade**, one for each decade. A three-decade counter is shown below. The inputs to the second and third decades come from Q8 of the previous decade. When Q8 in one decade goes from 1 to 0, it triggers the count for the next higher order decade while its own decade goes from 9 to 0.