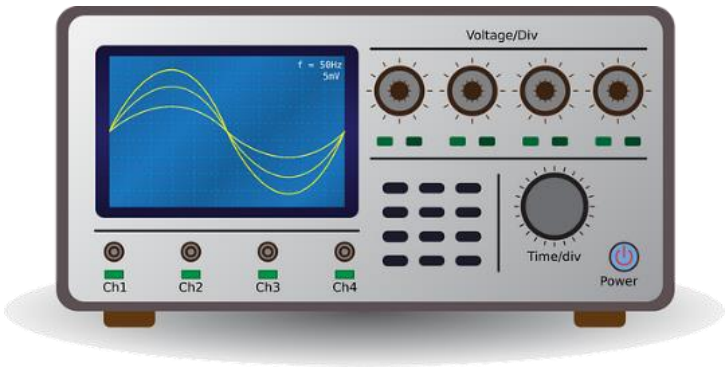
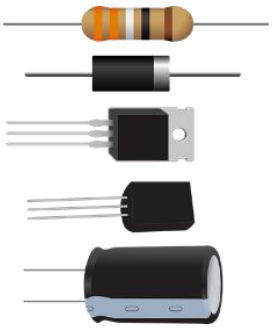
Salahaddin University-Erbil
College of Engineering
Electrical Engineering Department

Power Electronics

Electronics Lab





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Contents

Experiment No. 1

Adder and differential Amplifier

Introduction:

A differential input Op-Amp is a device with two input terminals, an output terminal and two power supply terminals. In addition, it will normally have terminals for offset balancing (for setting the output to zero when the input is zero) and may have terminal to which external components can be connected in order to modify the frequency response characteristics of the amplifier. The circuit symbol for an Op-Amp is a horizontal triangle. Op-Amps are used with dual power supplies consisting of a positive and negative supply in series connected as shown in figure 1.1.

The two input terminals of an op-amp are normally distinguished from each other symbolically by (+) and (-) sign. Input and output signals are measured with respect to the power supply common terminal which is normally earthen.

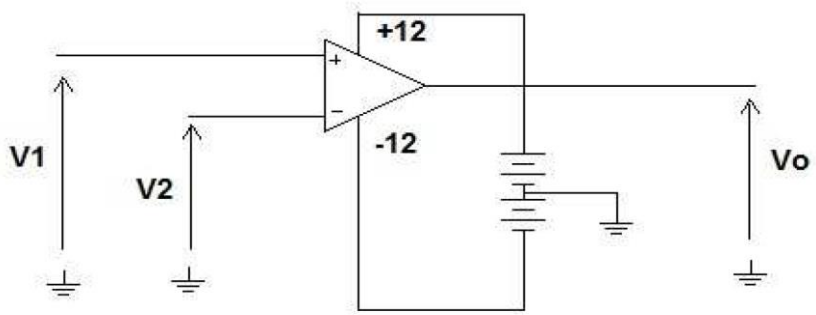

Figure 1.1

1.1 Adder Amplifier:

An adder is an electronic circuit that produces an output, which is equal to the sum of the applied inputs. An Op-Amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal. It is also called as a summing amplifier, since the output is an amplified one.

$$V_o = -(V_1 + V_2)$$

Verify this operation for the circuit shown in Figure 1.2 below if:

V_1	+5	+5	+5	2sin2000πt
V_2	+2	-2	2sin2000πt	2sin2000πt
V_o				

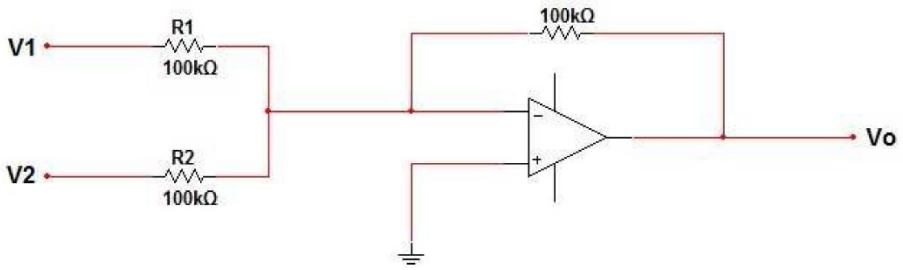

Figure 1.2

1.2 Differential Amplifier:

A differential amplifier is any tow-input amplifier that has an output proportional to the difference of the inputs.

Connect the circuit shown in figure 1.3. Then verify the operation of the circuit if

V_1	-5	-4.5	-2	+2	2
V_2	+4.5	+5	-3	+1.5	+3
V_o					

Note that

$$V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

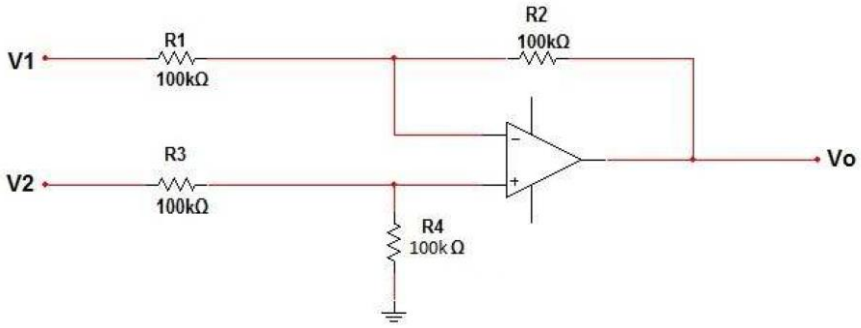

Figure 1.3

Discussion:

1. Design a circuit that subtract the value of two input and multiply the output by two.
2. How would you suggest a circuit that can add three inputs? Then drive the output voltage equation.

Experiment No. 2

Measurement of output resistance, input resistance, and CMRR in OP-AMP

2.1 Measurement of output resistance R_O

For the circuit shown in figure 2.1

a) Measure the V_{OL}
b) Connect a variable load resistance, R_L, to the output circuit.
c) Record the value of R_L when the $V_O = 1/2\ V_{OL}$, $R_O = R_{OL}$

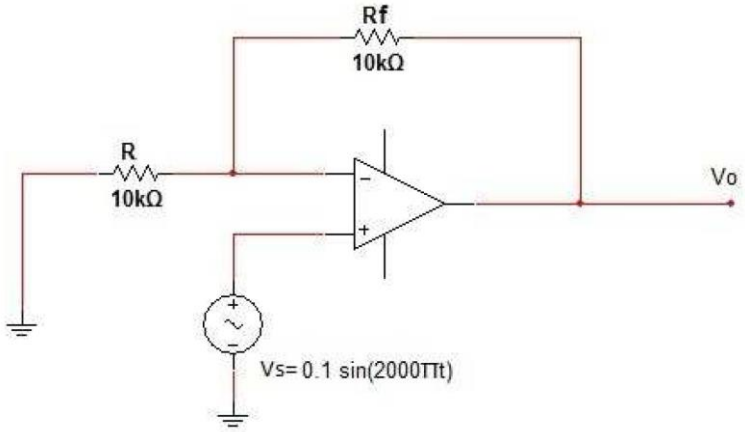

Figure 2.1

2.2 Measurement of input resistance R_{in}

a) While the power supply is off, construct the circuit shown in Figure 2.2.
b) Turn on the power supply, and set the sine-wave generator to 1KHz.
c) Adjust the sine-wave generator output amplitude for maximum undistorted signal at V_O.
d) Record the peak-to-peak value of V_{in}.
e) Place the oscilloscope Probe to position B. Adjust R_P until the peak-to-peak value of V_{in} is one-half the value recorded in step d.
f) Record the value of R_P. This resistance value is equal to input impedance of the op-amp, R_{in}.
g) Repeat step b through f for the following frequencies:
10Hz, 100Hz, and 100KHz.

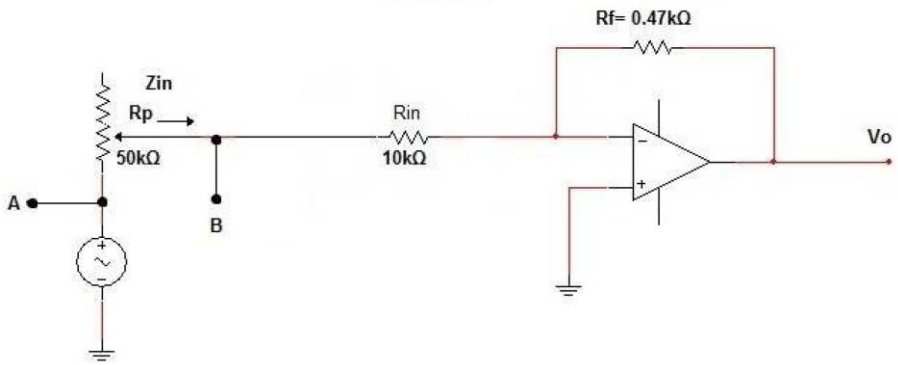

Figure 2.2

2.3 Measurement of Common Mode Rejection Ratio CMRR (ρ)

In electronics, the Common Mode Rejection Ratio CMRR of a differential amplifier (or other device) is a metric used to quantify the ability of the device to reject common-mode signals, i.e., those that appear simultaneously and in-phase on both inputs. In this part we will design the circuit to measure the CMRR of Op-Amp circuit.

a) Connect the circuit as shown in figure 2.3 if:
$R = R_1 = 100\Omega$
$R_f = R_1 = 100K\Omega$
$V_S = 0.1sin(2000\pi t)\ V$

b) Find the value of (ρ) if
$\rho = \frac{A_d}{A_c} = \frac{V_O}{V_{in}} / \frac{V_O}{V_C} = \frac{V_C}{V_{in}} = \frac{V_S}{V_{in}}$, while $\frac{V_O}{V_{in}} = \frac{R+R_f}{R}$
$\rho = \frac{R+R_f}{R} * \frac{V_S}{V_O}$

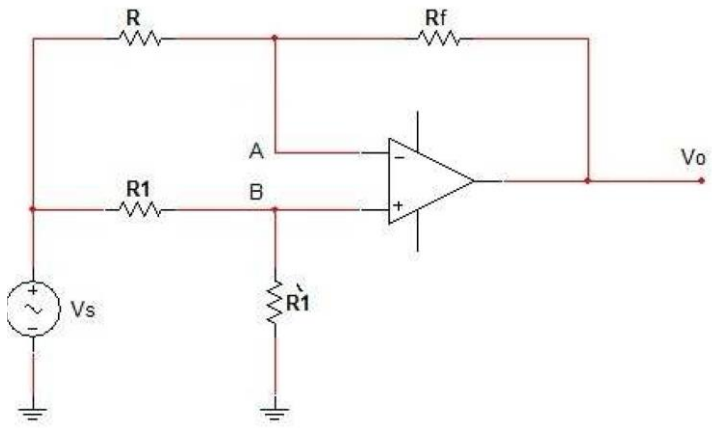

Figure 2.3

Discussion:

1. Ideally, how much is the output resistance of Op-Amp?
2. What is the input impedance of op-amp?
3. Does the input impedance change with different input signal frequencies?
4. How much is the common mode voltage gain, A_C of an op-amp?

Experiment No. 3

Sine Wave and Square Wave Generator

Introduction:

An wave generator or oscillator is a circuit that produces a periodic waveform on its output with only the dc supply voltage as an input. A repetitive input signal is not required except to synchronize oscillations in some applications. The output voltage can be either sinusoidal or non-sinusoidal, depending on the type of oscillator.

3.1 Sine-wave Generator

a) Connect the circuit as shown in figure 3.1.
b) Draw the output waveform.

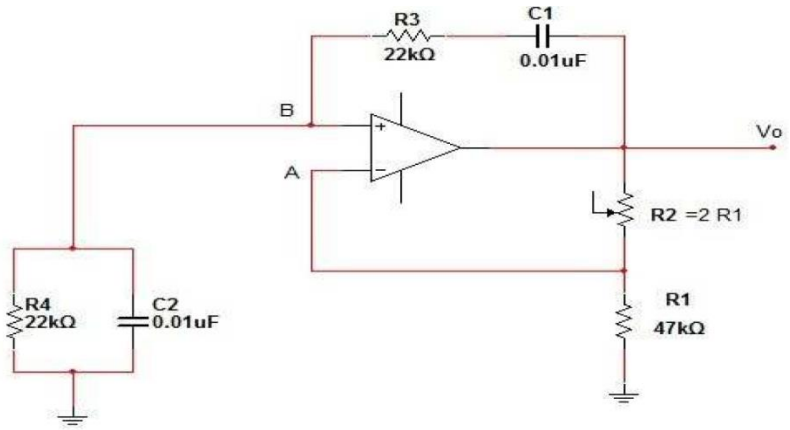

Figure 3.1

3.2 Square-wave Generator

a) Connect the circuit as shown in figure 3.2.
b) Draw V_A, V_B, V_O.
c) Measure T for the values shown in the table below

C (μF)	R_2 (KΩ)	R_3 (KΩ)	T (S)
0.01	100	220	
0.01	470	220	
0.01	20	220	

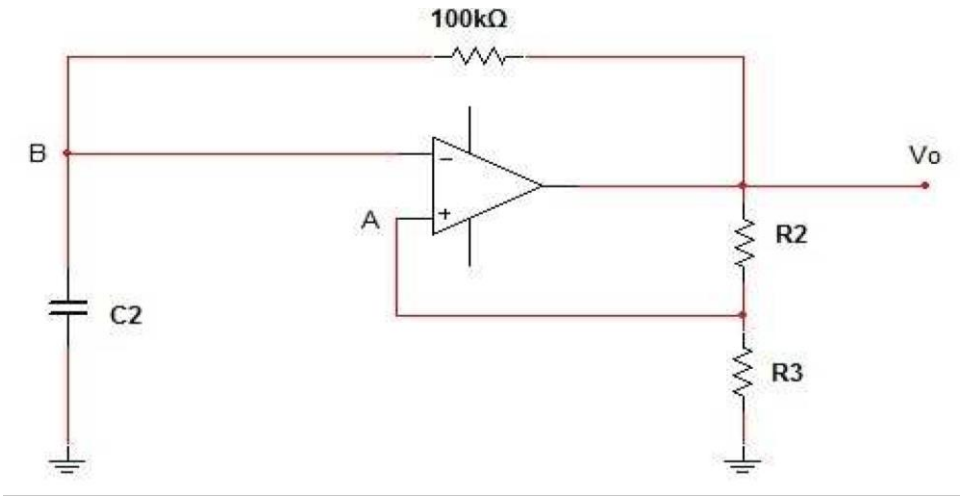

Figure 3.2

Discussion:

1. Derive the two conditions of sine-wave oscillation

   $V_A = V_B = \frac{1}{3}V_O$, and $F_O = \frac{1}{2\pi RC}$

2. In square-wave generator, derive the equation of (T) where

   $T = \frac{1}{F} = 2 * R_f * \ln\frac{1+\beta}{1-\beta}$, while $\beta = \frac{R_3}{R_2+R_3}$

Experiment No. 4

Active Low-Pass and High-Pass Filters

Introduction:

Filters are electronic circuits, which have the capability of selecting specific frequencies to pass to the output and blocking other frequencies. In other words, filters can be used to pass or amplify certain frequencies and block or attenuate other frequencies. Filters are usually categorized by the manner in which the output voltage varies with the frequency of the input voltage. The categories of active filters are low-pass, high-pass, band-pass, and band-stop. In this experiment we will build active low pass and active high pass filter.

2.1 Active Low-Pass Filter

Filters that use op-amps as the active element provide several advantages over passive filters (R, L, and C elements only). The op-amp provides gain, so the signal is not attenuated as it passes through the filter. The high input impedance of the op-amp prevents excessive loading of the driving source, and the low output impedance of the op-amp prevents the filter from being affected by the load that it is driving. Active filters are also easy to adjust over a wide frequency range without altering the desired response.

a) Connect the circuit shown in figure 4.1.
b) Change the frequency from (50Hz - 20KHz) and measure V_O.
c) Draw the frequency response curve then find the cut-off frequency
   Where: $F_c = 1/2\pi RC$

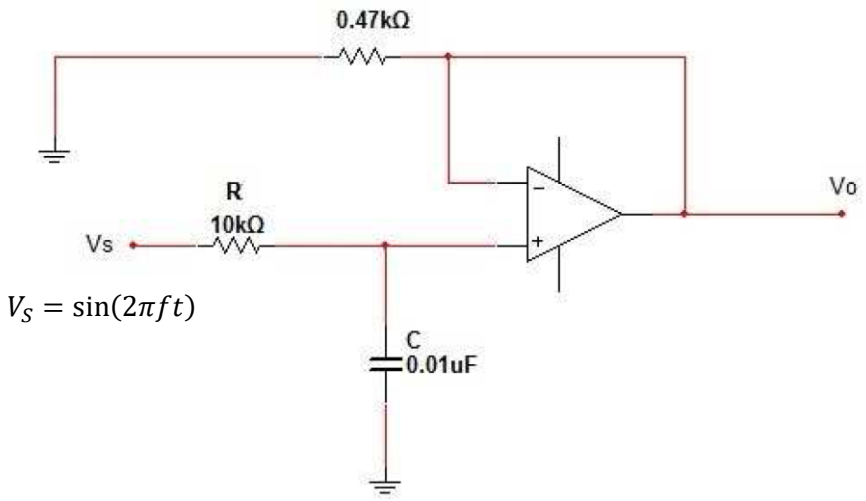

Figure 4.1

2.2 Active High-Pass Filter

In high-pass filters, the roles of the capacitor and resistor are reversed in the RC circuits. Otherwise, the basic parameters are the same as for the low-pass filters.

Repeat steps (a-c) of active low-pass filter circuit for the circuit shown in figure 4.2.

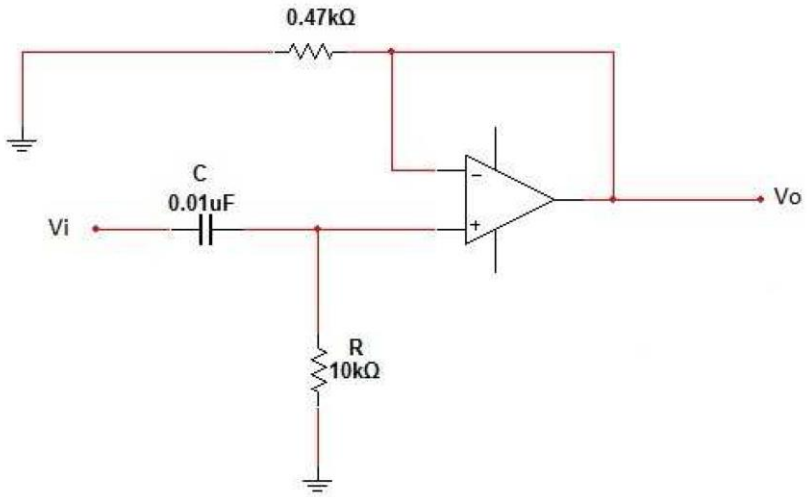

Figure 4.2

Discussion:

1. What is the different between passive and active filter?
2. Design a filter to have a cut-off frequency of (10KHz) and a gain of 3 for the pass band frequencies.

Experiment No. 5

Digital to Analog Convertor

Introduction:

A Digital-to-Analog Convertor (DAC or D/A Convertor) is an electronic circuit or a chip that is used to convert digital (usually binary) information or code (for example, from a CD or CD-ROM) into analog (usually a current or voltage) information (such as sound or audio signals). DAC chips are currently being used in many applications involving modern communication and instrumentation systems. For example, all digital synthesizers, samplers effect devices have DAC chips at their output to create audio signals.

There are two standard ways of building a digital-to-analog convertor:

a) Binary-weighted DAC.
b) R/2R Ladder DAC.

Both methods use operational amplifiers with negative feedback.

5.1 Binary-weighted DAC

In a binary-weighted-input DAC, shown in figure 5.1, the input current in each resistor is proportional to the column weight in the binary numbering system. It requires very accurate resistors. The MSB is represented by the large current, so it has the smallest resistor. To simplify analysis, assume all current goes through R_f and none into the Op-Amp. Therefore,

$$I_f = I_0 + I_1 + I_2 + I_3$$

$$V_{out} = I_f R_f$$

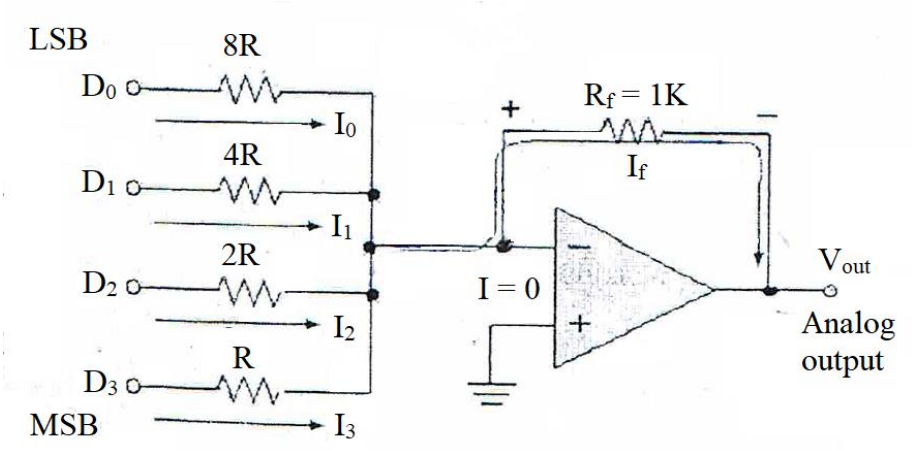

Figure 5.1

5.2 The R/2R Ladder DAC

The R/2R ladder requires only two values of resistors, shown in figure 5.2. By calculating a Thevenin equivalent circuit for each input, you can show that the output is proportional to the binary weight of inputs that are HIGH.

Each input that is HIGH contribute to the output by:

$$V_{out} = -\frac{V_s}{2^{n-i}}$$

where V_s = input HIGH level voltage
n = number of bits
i = bit number

For accuracy, the resistors must be precise ratios, which are easily done in integrated circuit. To obtain the total V_{out} the previous equation is applied to all inputs that are HIGH, then summing the results (applying Superposition Theorem).

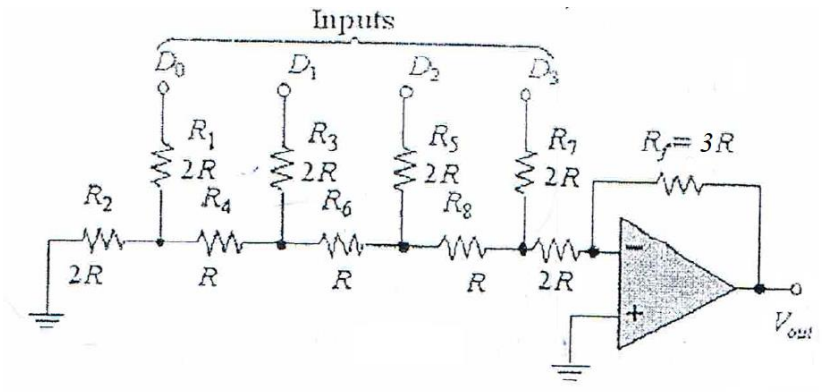

Figure 5.2

By direct circuit analysis, one can calculate the change in the output voltage contribution by each input. The results for our 4-bit circuit are shown in the table below.

Bit	Output voltage change, ΔV_{out}
D_3 (MSB)	$-V_s/2$
D_2	$-V_s/4$
D_1	$-V_s/8$
D_0 (LSB)	$-V_s/16$

Procedure:

1. Connect the DAC circuit of figure 5.1 choosing R as 0.625kΩ, 2R as 1.2kΩ, 4R as (2.2kΩ + 220Ω), and 8R as 4.7kΩ. Set the power supply voltage V_s = 5V.
2. Measure and record the actual values of the resistors used in your circuit.

3. Measure and record the value of the output Voltage V_{out} in each one of different switch combinations. Present your values in a table.
4. Repeat the above steps for the DAC circuit of Figure 5.2 choosing R as 4.7kΩ, 2R as 10kΩ, and 3R as 15kΩ.

Discussion:

1. Make a plot showing V_{out} versus the original inputs (x-axis) for both DAC circuits and using:
    - Original Calculations
    - Measured values
2. Did and of your measurements have more than 5% error? What was your maximum % error?
3. What sources of error may have contributed to the differences between theoretical values and measured values?
4. Other comments relevant to the experiment.

Experiment No. 6

Transistor as Switch

Introduction:

The BJT can be operated as a controlled switch that is the switch terminals are controlled by a signal at the third terminal. In addition, the BJT current gain allows a small input current to control a large switch current. When used as a switch the transistor operates in either the ON region or in OFF region and switches between the two. In the ON region the transistor acts as a very low resistance between collector & emitter (typically 1-50 Ω) in the OFF region the transistor acts as a very high resistance between collector & emitter (typically 10 MΩ). The transistor can be visualized as a perfect switch as shown in Figure 6.1. In analyzing switching circuits, a simple approximate method instead of using transistor curves is used as illustrated.

a) The ON condition: In Figure 6.2 the transistor will operate in ON state when a positive V_i is applied to the circuit to produce sufficient base current to saturate the transistor, the I_B and I_C can be evaluated as:

$$I_B\ min = (V_i - V_{BE})/R_B$$

and, $I_C = hfe * I_B$ in active region

When the transistor is fully saturated I_C will be:

$$I_C(sat) = V_{CC}/R_C$$

As I_B is increased from zero, the collector current increase proportionally until it reaches $I_C(sat)$ where further increase in I_B will not produce an increase in I_C which is saturated at the value $I_C(sat)$. the value of base current I_B that will cause saturation can be determined by:

$$I_B(sat) = I_C(sat)/hfe$$

b) The OFF condition: the transistor will be OFF whenever $I_B = 0$, In this case only a small leakage current will flow in the collector and emitter which can be neglected and all of V_{CC} appears across the collector and emitter.

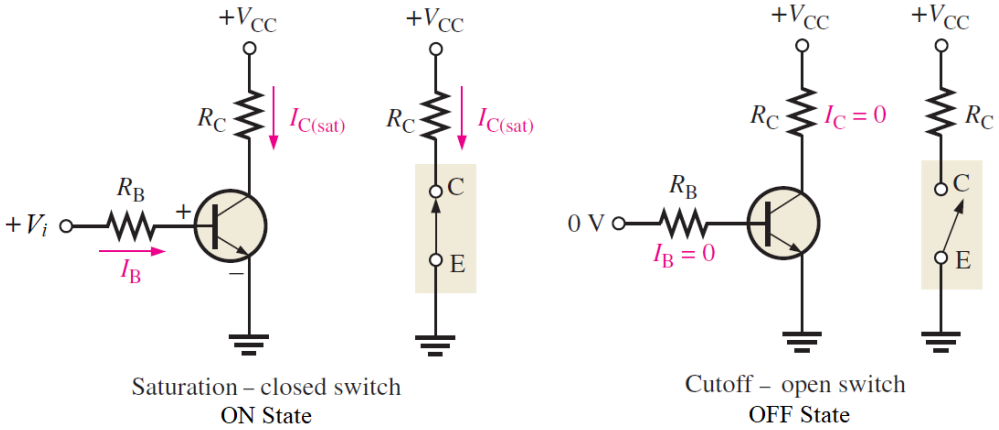

Figure 6.1

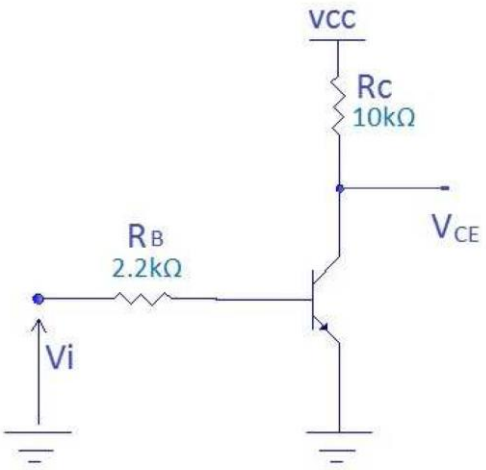

Figure 6.2

Transistor switching times

To see the behavior of transistor as it makes a transition from ON state to OFF state or vice versa consider the switch of Figure 6.2 driven by a pulse this wave form makes transition between voltage level V_{off} & V_{on} at V_{off} the transistor is at cutoff & at V_{on} the transistor is in saturation. The response of the collector voltage to the input is shown in Figure 6.3. When the input jumps to V_1 in order to turn the transistor on the charged junction capacitances (C_{BE}, C_{BC}) cause a delay. The output takes time to go from V_{CC} volt to Zero volts and the time that it takes the output to drop by 10% is called delay time (td) and the time it takes the output to drop an additional 80 % is called the fall time (tf) the sum td + tf is called the turn ON time (T_{ON}).

When the input drops to V_2 in order to turn transistor OFF once again the junction capacitance cause a delay in the transition when the transistor is saturated any base current above $I_B(sat)$ dose not produce an increase in I_C as a result is an excess of charges stored in the base region when the input tries to turn the transistor OFF the excess charges in the base are still available to produce collector current. As a result, collector saturation current keeps flowing until the excess base charges are completely removed. This time interval is called the storage time (ts) after the end of storage interval the transistor cannot turn OFF completely until C_{CB} charges to ($V_{CC} + V_2$) through R_C eventually the transistor ends up in the OFF state. The total turn OFF time (T_{OFF}) is the sum of ts and tr.

The faster (T_{ON}) requires a small (R_B) while a faster (T_{OFF}) requires a large value of (R_B). This problem can be solved by using **speed–up capacitors** across (R_B).

The ratio of the base current to the minimum base current required to put the transistor in saturation is called **over drive factor**.

Procedure:

1. Connect the circuit shown in Figure 6.2 with $R_C = 2.2K\Omega$, $R_B = 10K\Omega$, and 2SC945 transistor.
2. Find transfer characteristics (V_{CE} versus V_i) by applying an input voltage from (-5 to +5 volt in suitable steps), increase the measurement in the active region.
3. Measure the voltage (V_{BE}) required for saturation.

4. Apply a square wave of frequency 100kHz and 10 (V_{P-P}) to the input and draw the out put waveform under the input (together with the time relationship) and measure the switching times.
5. Decrease the input voltage to 6 (V_{P-P}) and observe the switching times, if there is any changes then record your observations.
6. Connect a (720 PF) capacitor in parallel with R_B and study its effect on the switching times.

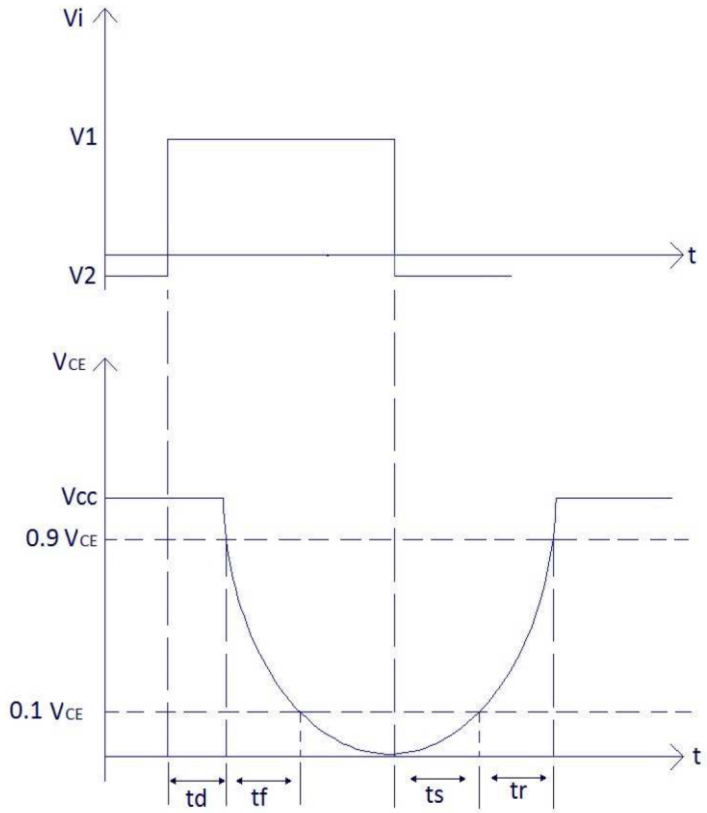

Figure 6.3

Discussion:

1. Measure the minimum base current required for saturation theoretically.
2. Measure the over drive factor when the input is 10 volts.
3. Discuss the effects of R_B and R_C on the value of (T_{ON}).
4. Discuss how to change R_B and R_C so that to reduce (T_{OFF}).