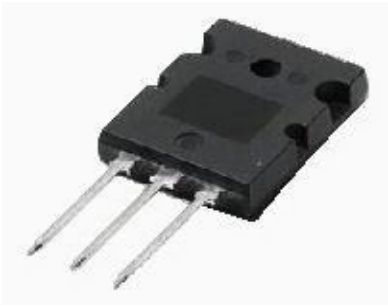
The Field Effect Transistor

Introduction:

The Field Effect Transistor or simply FET however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a "VOLTAGE" operated device.



Typical Field Effect Transistor

We remember from the previous tutorials that there are two basic types of Bipolar Transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. This is also true of FET's as there are also two basic classifications of Field Effect Transistor, called the N-channel FET and the P-channel FET.

The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and the Source terminals, which correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the "channel" which may be made of either a P-type or an N-type semiconductor material. The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are "Bipolar" devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a "Unipolar" device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

The Field Effect Transistor has one major advantage over its standard bipolar transistor cousins, in that their input impedance, (Rin) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

There are two main types of field effect transistor, the Junction Field Effect Transistor or JFET and the Insulated-gate Field Effect Transistor or IGFET), which is more commonly known as the standard Metal Oxide Semiconductor Field Effect Transistor or MOSFET for short.

The Junction Field Effect Transistor

We saw previously that a bipolar junction transistor is constructed using two PN-junctions in the main current carrying path between the Emitter and the Collector terminals. The Junction Field Effect Transistor (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high-resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively.

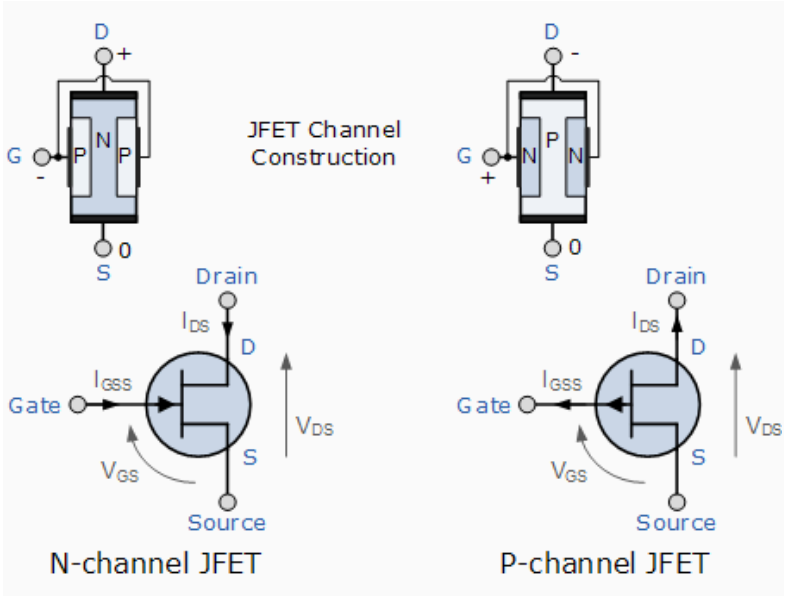
There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons. Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

We have said previously that there are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel. The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

Comparison of connections between a JFET and a BJT

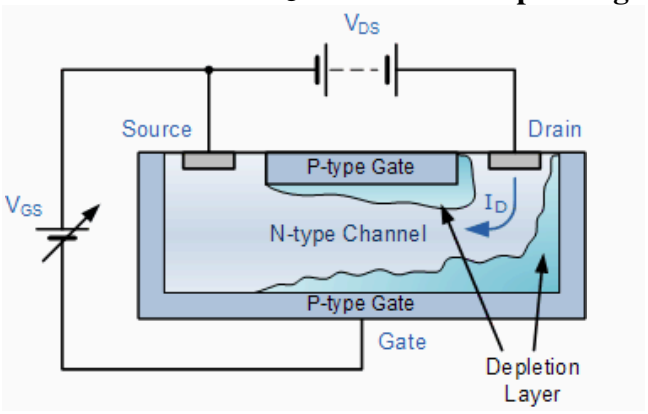
Bipolar Transistor		Field Effect Transistor
Emitter - (E)	>>	Source - (S)
Base - (B)	>>	Gate - (G)
Collector - (C)	>>	Drain - (D)

The symbols and basic construction for both configurations of JFETs are shown below.



The semiconductor "channel" of the Junction Field Effect Transistor is a resistive path through which a voltage V_{DS} causes a current I_D to flow. The JFET can conduct current equally well in either direction. A voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal. The PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias.
The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive. The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Bias arrangement for an N-channel JFET and corresponding circuit symbols.

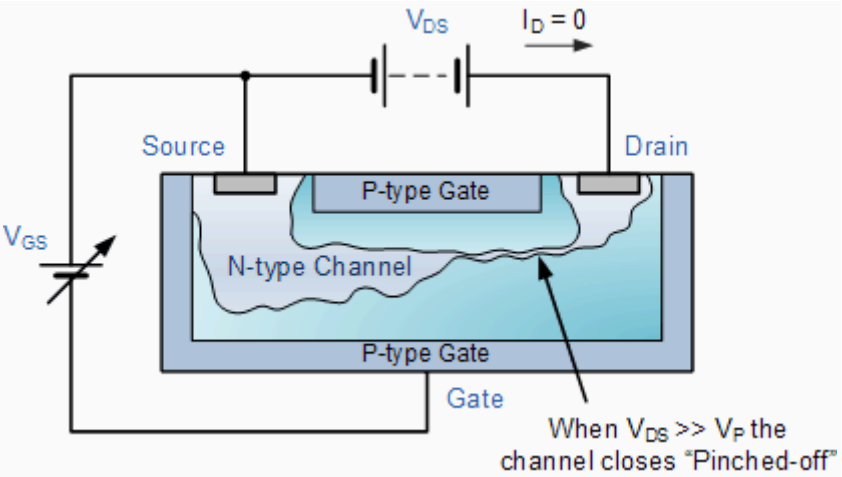


The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the depletion region around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices. This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself. The most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (i.e. the depletion region has near zero width).

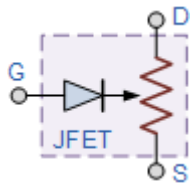
With no external Gate voltage ($V_G = 0$), and a small voltage (V_{DS}) applied between the Drain and the Source, maximum saturation current (I_{DSS}) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

If a small negative voltage ($-V_{GS}$) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel. Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ($-V_{GS}$) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the "pinch-off voltage", (V_P).

JFET Channel Pinched-off



In this pinch-off region the Gate voltage, V_{GS} controls the channel current and V_{DS} has little or no effect.



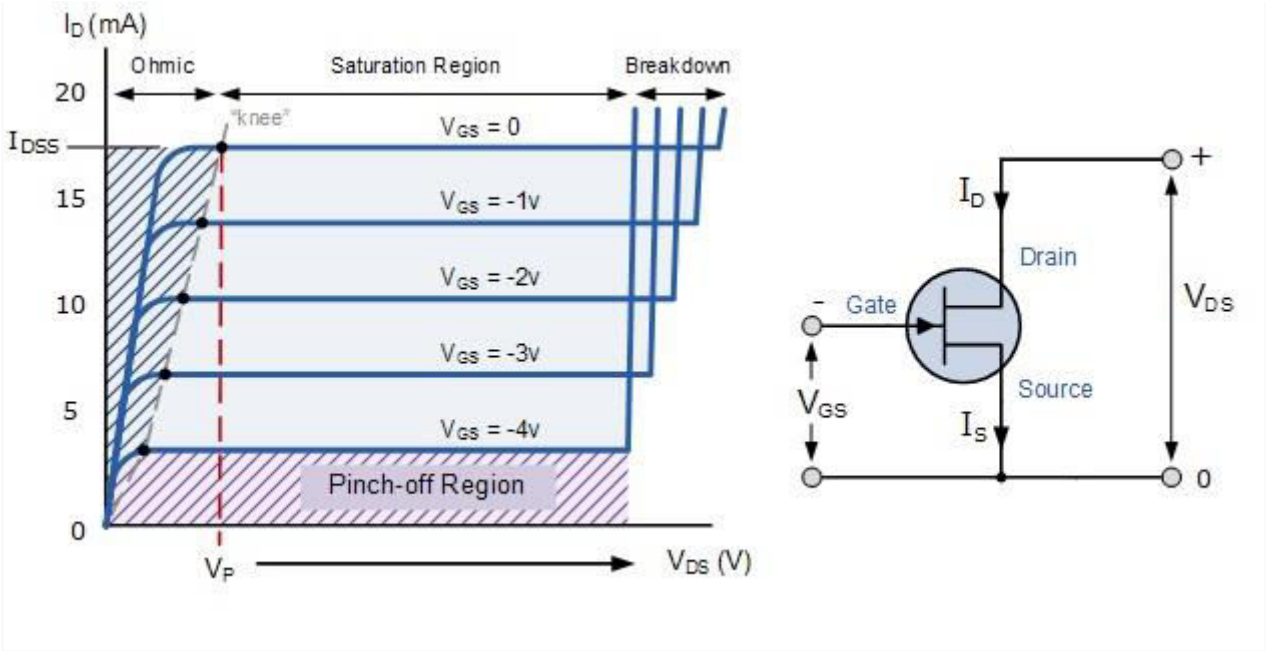
JFET Model

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when $V_{GS} = 0$ and maximum "ON" resistance (R_{DS}) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.
It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

No Gate voltage (V_{GS}) and V_{DS} is increased from zero.
No V_{DS} and Gate control is decreased negatively from zero.
V_{DS} and V_{GS} varying.

The P-channel Junction Field Effect Transistor operates the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.
The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as

Output characteristic V-I curves of a typical junction FET.



The voltage V_{GS} applied to the Gate controls the current flowing between the Drain and the Source terminals. V_{GS} refers to the voltage applied between the Gate and the Source while V_{DS} refers to the voltage applied between the Drain and the Source. Because a Junction Field Effect Transistor is a voltage controlled device, "NO current flows into the gate!" then the Source current (I_S) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

Ohmic Region - When $V_{GS} = 0$ the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

Cut-off Region - This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.

Saturation or Active Region - The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.

Breakdown Region - The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.
The Drain current is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

Drain current in the active region.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and I_{DSS} (maximum current). By knowing the Drain current I_D and the Drain-Source voltage V_{DS} the resistance of the channel (I_D) is given as:

Drain-Source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: gm is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

JFET Amplifier

Just like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R_1 and R_2 as shown.

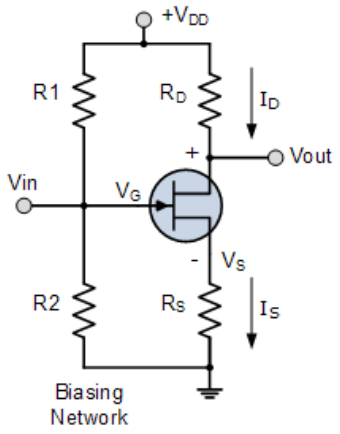
Biasing of JFET Amplifier

$$V_S = I_D R_S = \frac{V_{DD}}{4}$$

$$V_S = V_G - V_{GS}$$

$$V_G = \left(\frac{R2}{R1 + R2} \right) V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$



This common source (CS) amplifier circuit is biased in class A mode by the voltage divider network formed by R_1 and R_2. The voltage across the Source resistor RS is generally set at one fourth V_{DD}, (V_{DD} /4). The required Gate voltage can then be calculated using this RS value. Since the Gate current is zero, ($I_G = 0$) we can set the required DC quiescent voltage by the proper selection of resistors R_1 and R_2.

The control of the Drain current by a negative Gate potential makes the Junction Field Effect Transistor useful as a switch and it is essential that the Gate voltage is never positive for an N-channel JFET as the channel current will flow to the Gate and not the Drain resulting in damage to the JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

Differences between a FET and a Bipolar Transistor

Field Effect Transistors can be used to replace normal Bipolar Junction Transistors in electronic circuits and a simple comparison between FET's and transistors stating both their advantages and their disadvantages is given below.

	Field Effect Transistor (FET)	Bipolar Junction Transistor (BJT)
1	Low voltage gain	High voltage gain
2	High current gain	Low current gain
3	Very input impedance	Low input impedance
4	High output impedance	Low output impedance
5	Low noise generation	Medium noise generation
6	Fast switching time	Medium switching time
7	Easily damaged by static	Robust
8	Some require an input to turn it "OFF"	Requires zero input to turn it "OFF"
9	Voltage controlled device	Current controlled device
10	Exhibits the properties of a Resistor	
11	More expensive than bipolar	Cheap
12	Difficult to bias	Easy to bias

Basic electronic circuits

JFET characteristic

Object of the experiment:

Transistor current-voltage (I-V) characteristics of Field Effect Transistor (FET) circuit are investigated. The characteristics are derived using current and voltage measurements.

Apparatus:

1 DC power supply HY3002-2
1 JFET Transistor (k105) …NPN
1 plug-in board A4
2 resistances (4.7KΩ, 2.2KΩ)
10 pairs of cables, 50 cm, red/blue

Set up:

Theory:

The drain characteristics for a typical N-channel FET given by $I_D=(V_{DS}),V_{GS}$=constant for V_{GS}=0 and when V_{DS} is zero the channel is entirely open for small applied voltage V_{DS} the N types bar acts as a simple semiconductor resistor and I_D increase linearly with V_{DS} , this region is called ohmic region , for V_{DS} is greater than a few volts the n-type region near the drain is reverse biased relative to the p type gate therefore the width near the drain increases constricting the width of the N-channel .As we increase V_{DS} further the channel width approaches zero (but still finite) . This is called pinch off region the current I_D begins to level off and approaches a constant value . The voltage V_{DS} at which pinch off occurs is called pinch off voltage V_P. The current I_D at the pinch off point when V_{GS} =0 is denoted by I_{DSS}. If now a gate voltge V_{GS} is applied (in a direction to provide additional reveres bias –G is made negative relative to the source S) pinch off will occur at smaller voltage of VDS and the maximum drain current IDS (sat) will be smaller .

The important parameters of JFET are defined as follow:

1- Drain dynamic resistance $rd = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ =\ \text{constant}}$,

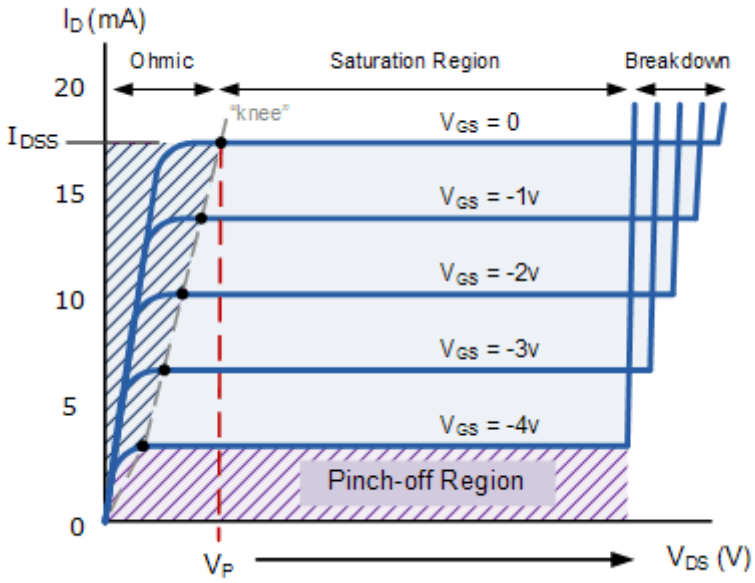
2- The output conductor $g_0=\frac{1}{r_d}$

3- Mutual conductor (or transconductance) $gm = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}\ =\ constant}$

4- Amplifier factor $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D\ =\ constant}$

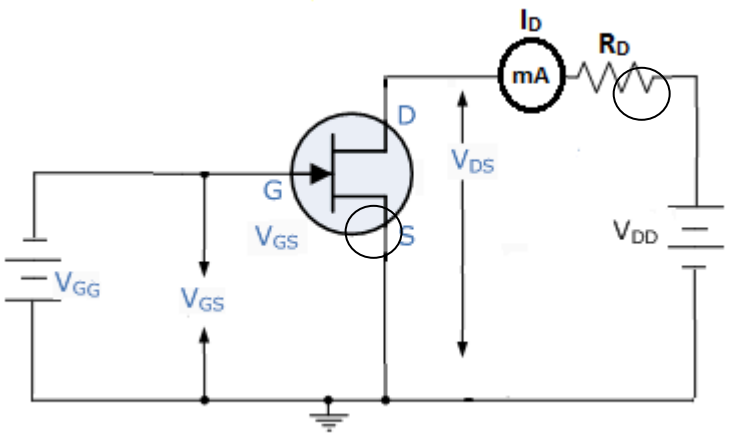
These parameters are related by the equation

$$\mu = rd \times gm$$



Procedure:

1- Connect the circuit as shown in the figure be



2- Let V_{GS} = 0.5V, increase V_{DS} in steps record I_D and V_{DS} in each step
3- Repeat as in 2 above for V_{GS} = -1,-2,-3 V(increase V_{GS} to the number that make I_D to zero) , tabulate the results as below:

V_{DS}/V	V_{GS}=0.5/V	V_{GS}=-1/V	V_{GS}=-1.5/V	V_{GS}=-2/V
	I_D/mA	I_D/mA	I_D/mA	I_D/mA
9				
8				
7				
6				
5				
4				
3				
2				
1				
0.9				
0.7				
0.5				
0.3				
0.1				
0				

4- Plot the drain characteristic I_D=f(V_{DS}) at fixed V_{GS}
5- From the plot calculate r_d , gm and μ at a suitable operation point.

Basic electronic circuits

JFET Amplifier

Object of the experiment:

To measure the frequency response for (JFET):

A- Common Source

B- Common Drain

Apparatus:

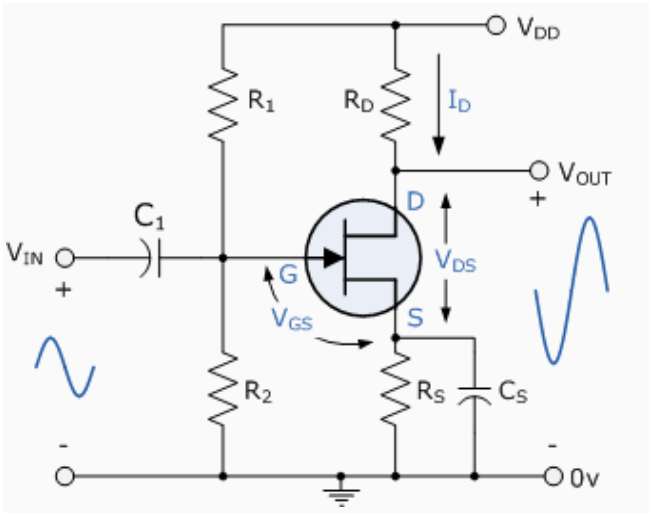
1 DC power supply HY3002-2
1 AC 1TRIO audio generator AG202A
1 JFET Transistor (k105) …NPN
1 plug-in board A4
4 resistances (4.7KΩ, 2.2KΩ, KΩ, 1μΩ)
3 capacitors (2μf,32μf, 2μf)
10 pairs of cables, 50 cm, red/blue

Set up:

Theory:

So far we have looked at the bipolar type transistor amplifier and especially the common emitter amplifier, but small signal amplifiers can also be made using Field Effect Transistors or FET's for short. These devices have the advantage over bipolar transistors of having an extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals. The design of an amplifier circuit based around a junction field effect transistor or "JFET", (n-channel FET for this tutorial) or even a metal oxide silicon FET or "MOSFET" is exactly the same principle as that for the bipolar transistor circuit used for a Class A amplifier circuit we looked at in the previous tutorial. Firstly, a suitable quiescent point or "Q-point" needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices. These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. In this tutorial we will look at the Common Source JFET Amplifier as this is the most widely used JFET amplifier design. Then consider the common source JFET amplifier circuit below.

A- Common Source JFET Amplifier



The amplifier circuit consists of an N-channel JFET, but the device could also be an equivalent N-channel depletion-mode MOSFET as the circuit diagram would be the same just a change in the FET, connected in a common source configuration. The JFET gate voltage V_g is biased through the potential divider network set up by resistors R_1 and R_2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor. Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required. We can compare the JFET to the bipolar junction transistor (BJT) in the following table.

JFET to BJT Comparison

JFET	BJT
Gate, (*G*)	Base, (*B*)
Drain, (*D*)	Collector, (*C*)
Source, (*S*)	Emitter, (*E*)
Gate Supply, (V_G)	Base Supply, (V_B)
Drain Supply, (V_{DD})	Collector Supply, (V_{CC})
Drain Current, (i_D)	Collector Current, (i_C)

Since the N-Channel JFET is a depletion mode device and is normally "ON", a negative gate voltage with respect to the source is required to modulate or

control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self biasing

arrangement as long as a steady current flows through the JFET even when there is no input signal present and Vg maintains a reverse bias of the gate-source pn junction. In this example the biasing is provided from a potential divider network allowing the input signal to produce a voltage fall at the gate as well as voltage rise at the gate with a sinusoidal signal. Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage V_G is given as:

$$V_G = \frac{V_{DD}\,R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Note that this equation only determines the ratio of the resistors R_1 and R_2, but in order to take advantage of the very high input impedance of the JFET as well as reducing the power dissipation within the circuit, we need to make these resistor values as high as possible, with values in the order of 1 to 10MΩ being common.The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, R_d. The output voltage, V_{out} is developed across this load resistance. The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, R_s included in the source lead with the same drain current flowing through this resistor. Resistor, R_s is also used to set the JFET amplifiers "Q-point".

When the JFET is switched fully "ON" a voltage drop equal to R_s x I_D is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across R_s due to the drain current provides the necessary reverse biasing condition across the gate resistor, R_2 effectively generating negative feedback. In order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, V_g. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, I_S as "No Current" enters the Gate terminal and this can be given as:

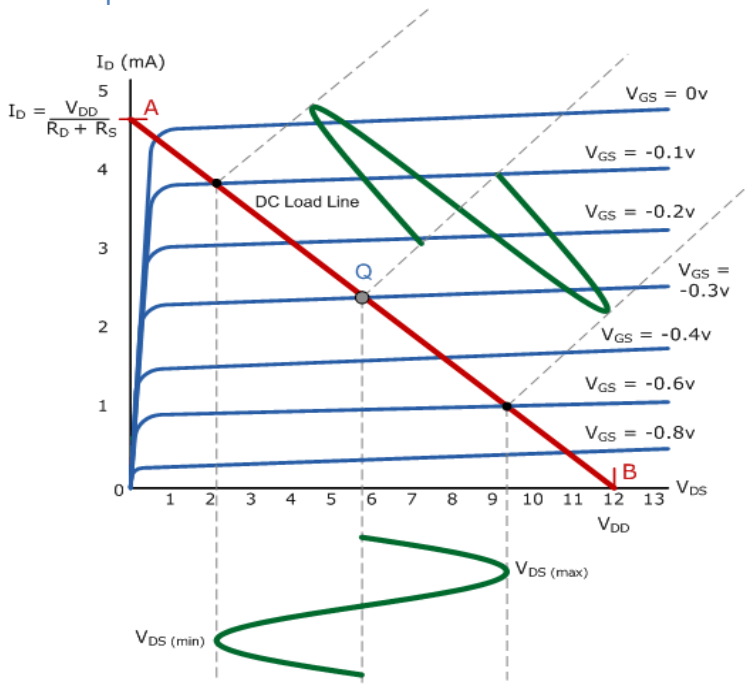
$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, R_s and the source by-pass capacitor, C_s serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to Provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across Rs.

The the value in farads of the source by-pass capacitor is generally fairly high above 100uF and will be polarized. This gives the capacitor an impedance value much smaller, less than 10% of the transconductance, gm (the transfer coefficient representing gain) value of the device. At high frequencies the by-pass capacitor acts essentially as a short-circuit and the source will be effectively connected directly to ground.

The basic circuit and characteristics of a Common Source JFET Amplifier are very similar to that of the common emitter amplifier. A DC load line is constructed by joining the two points relating to the drain current, Id and the supply voltage, V_{DD} remembering that when Id = 0: (V_{DD}= V_{DS}) and when Vds = 0: ($I_D = V_{DD}/R_L$). The load line is therefore the intersection of the curves at the Q-point as follows.

Common Source JFET Amplifier Characteristics Curves



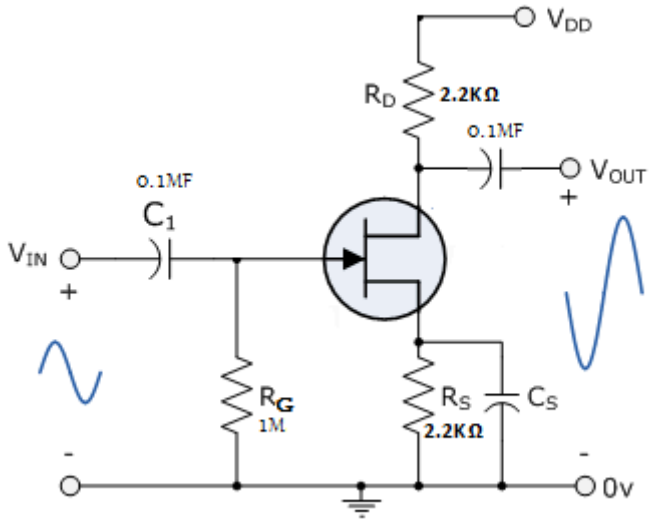
As with the common emitter bipolar circuit, the DC load line for the common source JFET amplifier produces a straight line equation whose gradient is given as: $-1/(R_d + Rs)$ and that it crosses the vertical Id axis at point A equal to $V_{DD}/(R_D + Rs)$. The other end of the load line crosses the horizontal axis at point B which is equal to the supply voltage, V_{DD}. The actual position of the Q-point on the DC load line is generally positioned at the mid centre point of the load line (for class-A operation) and is determined by the mean value of Vg which is biased negatively as the JFET is a depletion-mode device. Like the bipolar common emitter amplifier the output of the Common Source JFET Amplifier is 180 degree out of phase with the input signal.

One of the main disadvantages of using Depletion-mode JFET is that they need to be negatively biased. Should this bias fail for any reason the gate-source voltage may rise and become positive causing an increase in drain current resulting in failure of the drain voltage, V_D. Also the high channel resistance, $R_{DS}(on)$ of the junction FET, coupled with high quiescent steady state drain current makes these devices run hot so additional heat sink is required. However, most of the problems associated with using JFET's can be greatly reduced by using enhancement-mode MOSFET devices instead. MOSFETs or Metal Oxide Semiconductor FET's have much higher input impedances and low channel resistances compared to the equivalent JFET. Also the biasing arrangements for MOSFETs are different and unless we bias them positively for N-channel devices and negatively for P-channel devices no drain current will flow, then we have in effect a failsafe transistor.

Procedure:

A- Common source (CS) amplifier:

1- Connect the circuit as shown in the finger: (C_s disconnected)



2- Drive the amplifier with a small (10mV) sine wave of 1 KHz. Look at υ_{in} and υ_{out}.(if there is distortion decrease υ_{in})

3- Measure the frequency response of the amplifier starting from 20 HZ. Change the test frequency to cover the upper cut-off frequency response apply low in put signal levels (in order of few mille-volts) to ensure that the output signal is not distorted .monitor both input and output waveforms on the oscilloscope put your result in the table :

f/HZ	Log f/HZ	v_{in}/V	v_{out}/V	$Av = v_{0ut}/ v_{in}$
20	1.30103			
40	1.60206			
60	1.778151			
80	1.90309			
100	2			
200	2.30103			
400	2.60206			
600	2.778151			
800	2.90309			
1000	3			
2000	3.30103			
4000	3.60206			
6000	3.778151			
8000	3.90309			
10000	4			
20000	4.30103			
40000	4.60206			
60000	4.778151			
80000	4.90309			
100000	5			
120000	5.079181			
140000	5.146128			
160000	5.20412			
180000	5.255273			
200000	5.30103			

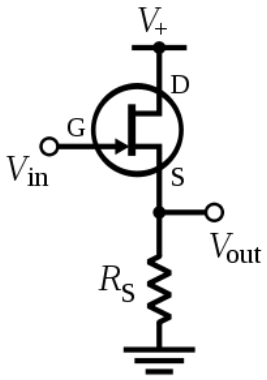
4- Repeat number (3) after Connect the capacitor (C_s=2μF) across R_s and measure the frequency response for same range .
5- Plot the frequency response for both case in the same graph to compare between them

B-common-drain amplifier :

In electronics, a common-drain amplifier, also known as a source follower, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier.

In addition, this circuit is used to transform impedances. For example, the Thévenin resistance of a combination of a voltage follower driven by a voltage source with high Thévenin resistance is reduced to only the output resistance of the voltage follower, a small resistance. That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a driving stage and a high load (ie a low resistance) presents an infinite resistance (low load) to the driving stage, an advantage in coupling a voltage signal to a large load.

Characteristics



Basic N-channel JFET source follower circuit (neglecting biasing details).

At low frequencies, the source follower pictured at right has the following small signal characteristics. Voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_m R_S}{g_m R_S + 1} \approx 1 \qquad (g_m R_S \gg 1)$$

Current gain:

$$A_i = \infty$$

Input impedance:

$$r_{\text{in}} = \infty$$

Output impedance: (the parallel notation $A \| B$ indicates the impedance of components A and B that are connected in parallel)

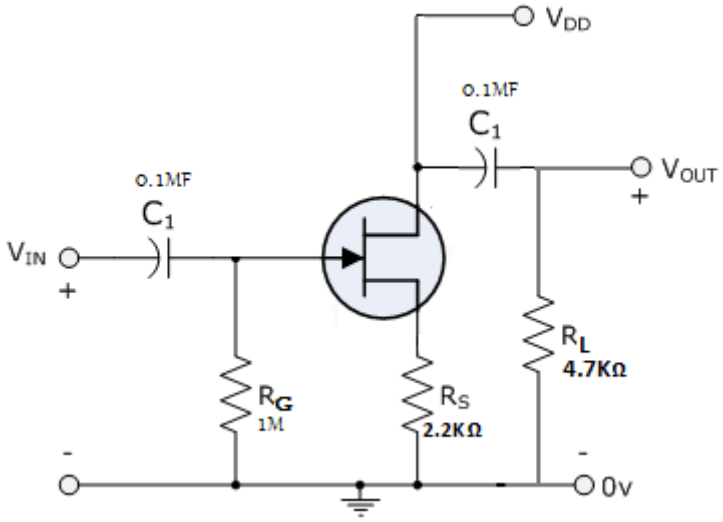
$$r_{\text{out}} = R_S \| \frac{1}{g_m} = \frac{\frac{R_S}{g_m}}{R_S + \frac{1}{g_m}} = \frac{R_S}{g_m R_S + 1} \approx \frac{1}{g_m} \qquad (g_m R_S \gg 1)$$

The variable g_m that is not listed in Figure 1 is the transconductance of the device (usually given in units of Siemens).

Procedure:

Common drain (CD) amplifier:

1- Connect the circuit as shown in the finger: (C_s disconnected)



2- Drive the amplifier with a small signal (10mV) sine wave of 1 KHz. measure υ_{in} Aυ for f= 1KHz and f=100Khz (if there is distortion decrease υ_{in})

2- Measure the frequency response of the amplifier starting from 20 HZ. Change the test frequency to cover the upper cut-off frequency response apply low in put signal levels (in order of few mille-volts) to ensure that the output signal is not distorted .monitor both input and output waveforms on the oscilloscope put your result in the table :

f/HZ	Log f/HZ	v_{in}/V	v_{out}/V	$Av = v_{0ut}/ v_{in}$
20	1.30103			
40	1.60206			
60	1.778151			
80	1.90309			
100	2			
200	2.30103			
400	2.60206			
600	2.778151			
800	2.90309			
1000	3			
2000	3.30103			
4000	3.60206			
6000	3.778151			
8000	3.90309			
10000	4			
20000	4.30103			
40000	4.60206			
60000	4.778151			
80000	4.90309			
100000	5			
120000	5.079181			
140000	5.146128			
160000	5.20412			
180000	5.255273			
200000	5.30103			

3- Repeat number (3) after Connect the capacitor (C_s=2μF) across R_s and measure the frequency response for same range .
4- Plot the frequency response for both case in the same graph to compare between them

Ideal Operational Amplifiers

Introduction

Operational Amplifiers in general

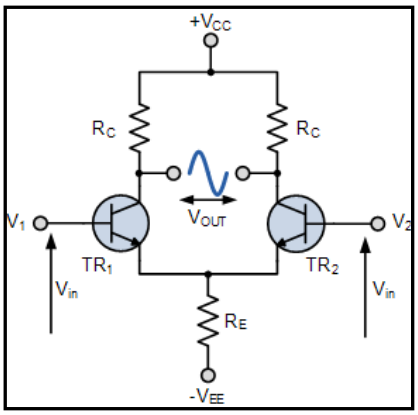
As well as resistors and capacitors, **Operational Amplifiers**, or **Op-amps** as they are more commonly called, are one of the basic building blocks of Analogue Electronic Circuits. Operational amplifiers are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation. An ideal Operational Amplifier is basically a three-terminal device which consists of two high impedance inputs, one called the Inverting Input, marked with a negative sign, ("-") and the other one called the Non-inverting Input, marked with a positive plus sign ("+").

The third terminal represents the op-amps output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

- Voltage – Voltage "in" and Voltage "out"
- Current – Current "in" and Current "out"
- Transconductance – Voltage "in" and Current "out"
- Transresistance – Current "in" and Voltage "out"

Differential Amplifier

The circuit below shows a generalized form of a differential amplifier with two inputs marked V_1 and V_2. The two identical transistors TR_1 and TR_2 are both biased at the same operating point with their emitters connected together and returned to the common rail, $-V_{EE}$ by way of resistor R_e.

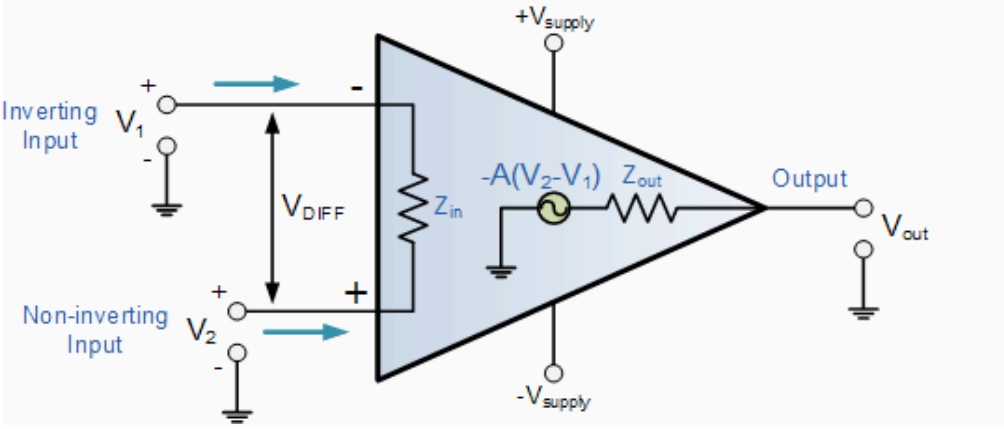


The circuit operates from a dual supply $+V_{CC}$ and $-V_{EE}$ which ensures a constant supply. The voltage that appears at the output, V_{out} of the amplifier is the difference between the two input signals as the two base inputs are in *anti-phase* with each other. So as the forward bias of transistor, TR_1 is increased, the forward bias of transistor TR_2 is reduced and vice versa. Then if the two transistors are perfectly matched, the current flowing through the common emitter resistor, R_E will remain constant.

Like the input signal, the output signal is also balanced and since the collector voltages either swing in opposite directions (anti-phase) or in the same direction (in-phase) the output voltage signal, taken from between the two collectors is, assuming a perfectly balanced circuit the zero difference between the two collector voltages. This is known as the Common Mode of Operation with the common mode gain of the amplifier being the output gain when the input is zero. Ideal Operational Amplifiers also have one output (although there are ones with an additional differential output) of low impedance that is referenced to a common ground terminal and it should ignore any common mode signals that is, if an identical signal is applied to both the inverting and non-inverting inputs there should no change to the output. However, in real amplifiers there is always some variation and the ratio of the change to the output voltage with regards to the change in the common mode input voltage is called the **Common Mode Rejection Ratio** or **CMRR**.

Operational Amplifiers on their own have a very high open loop DC gain and by applying some form of **Negative Feedback** we can produce an operational amplifier circuit that has a very precise gain characteristic that is dependant only on the feedback used. An operational amplifier only responds to the difference between the voltages on its two input terminals, known commonly as the "*Differential Input Voltage*" and not to their common potential. Then if the same voltage potential is applied to both terminals the resultant output will be zero. An Operational Amplifiers gain is commonly known as the Open Loop Differential Gain, and is given the symbol (A_o).

Equivalent Circuit for Ideal Operational Amplifiers



Op-amp Idealized Characteristics

PARAMETER	IDEALIZED CHARACTERISTIC
Open Loop Gain, (Av_o)	Infinite - The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. Open-loop gain is the gain of the op-amp without positive or negative feedback and for an ideal amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.
Input impedance, (Z_{in})	Infinite - Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry (I_{in} =0). Real op-amps have input leakage currents from a few pico-amps to a few milli-amps.
Output impedance, (Z_{out})	Zero - The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output-impedance in the 100-20Ω range.
Bandwidth, (BW)	Infinite - An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.
Offset Voltage, (V_{io})	Zero - The amplifiers output will be zero when the voltage difference between the inverting and the non-inverting inputs is zero, the same or when both inputs are grounded. Real op-amps have some amount of output offset voltage.

From these "idealized" characteristics above, we can see that the input resistance is infinite, so no current flows into either input terminal (the "current rule") and that the differential input offset voltage is zero (the "voltage rule"). It is important to remember these two properties as they will help us understand the workings of the **Operational Amplifier** with regards to the analysis and design of op-amp circuits.

However, real **Operational Amplifiers** such as the commonly available uA741, for example do not have infinite gain or bandwidth but have a typical "Open Loop Gain" which is defined as the amplifiers output amplification without any external feedback signals connected to it and for a typical operational amplifier is about 100dB at DC (zero Hz). This output gain decreases linearly with

frequency down to "Unity Gain" or 1, at about 1MHz and this is shown in the following open loop gain response curve.

Open-loop Frequency Response Curve

From this frequency response curve we can see that the product of the gain against frequency is constant at any point along the curve. Also that the unity gains (0dB) frequency also determines the gain of the amplifier at any point along the curve. This constant is generally known as the Gain Bandwidth Product or GBP.

Therefore, **GBP = Gain x Bandwidth or A x BW**.

The Voltage Gain (A) of the amplifier can be found using the following formula:

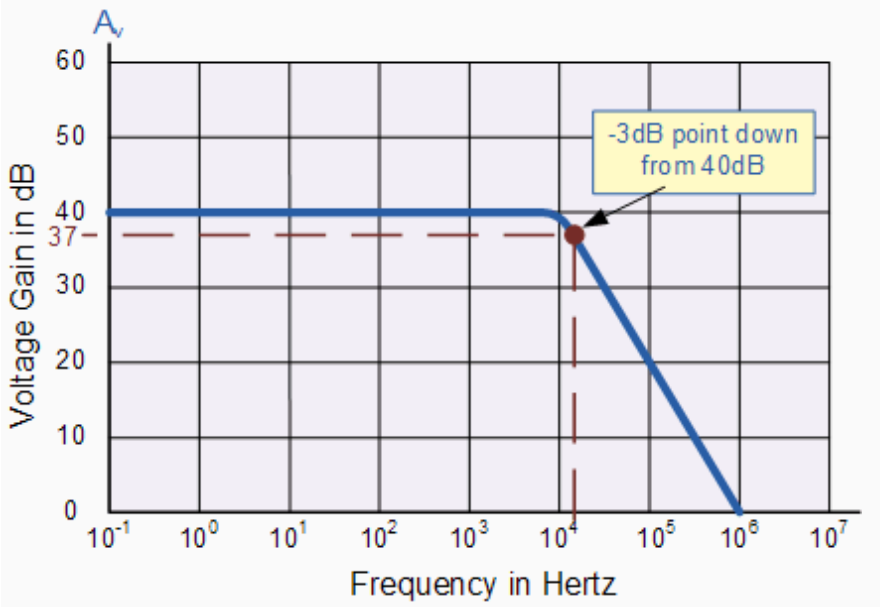
$$\text{Voltage Gain, (A)} = \frac{V_{out}}{V_{in}}$$

and in Decibels or (dB) is given as:

$$20\log(A) \text{ or } 20\log\frac{V_{out}}{V_{in}} \textit{ in dB}$$

An Operational Amplifiers Bandwidth

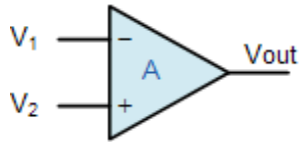
The operational amplifiers bandwidth is the frequency range over which the voltage gain of the amplifier is above 70.7% or -**3dB** (where 0dB is the maximum) of its maximum output value as shown below.



Here we have used the 40dB line as an example. The -3dB or 70.7% of V_{max} down point from the frequency response curve is given as 37dB. Taking a line across until it intersects with the main GBP curve gives us a frequency point just above the 10kHz line at about 12 to 15kHz. We can now calculate this more accurately as we already know the GBP of the amplifier, in this particular case 1MHz.

Operational Amplifiers Summary

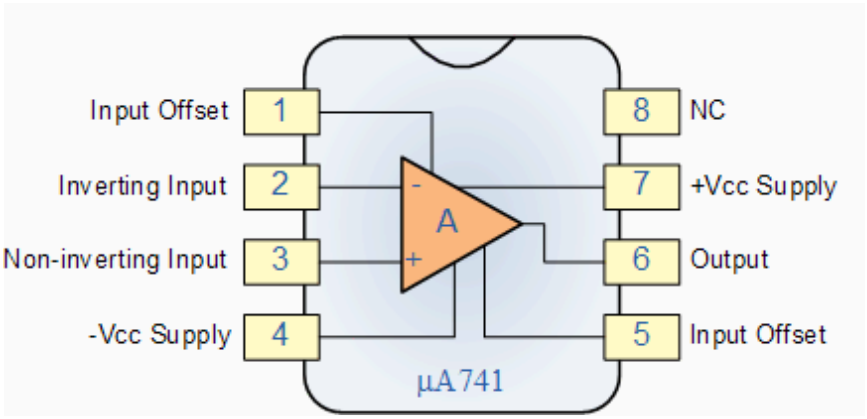
We know now that an **Operational amplifiers** is a very high gain DC differential amplifier that uses one or more external feedback networks to control its response and characteristics. We can connect external resistors or capacitors to the op-amp in a number of different ways to form basic "building Block" circuits such as, Inverting, Non-Inverting, Voltage Follower, Summing, Differential, Integrator and Differentiator type amplifiers.



Op-amp Symbol

An "ideal" or perfect Operational Amplifier is a device with certain special characteristics such as infinite open-loop gain A_o, infinite input resistance Rin, zero output resistance R_{out}, infinite bandwidth 0 to ∞ and zero offset (the output is exactly zero when the input is zero).

There are a very large number of operational amplifier I_C's available to suit every possible application from standard bipolar, precision, high-speed, low-noise, high-voltage, etc in either standard configuration or with internal JFET transistors. Operational amplifiers are available in I_C packages of single, dual or quad op-amps within one single device. The most commonly available and used of all operational amplifiers in basic electronic kits and projects is the industry standard μA-741.



EXP.NO.14
Physics experiments
3rd stage

Application operation amplifier

Inverting Amplifier

Object of the experiment:

Study the inverting amplifier (gain and bandwidth)

Apparatus:

1 DC power supply HY3002-2
1TRIO audio generator AG202A
1 operation amplifier LM741
1 plug-in board A4
2 resistance (1KΩ,10KΩ,100KΩ,…..
10 pairs of cables, 50 cm, red/blue

Set up:

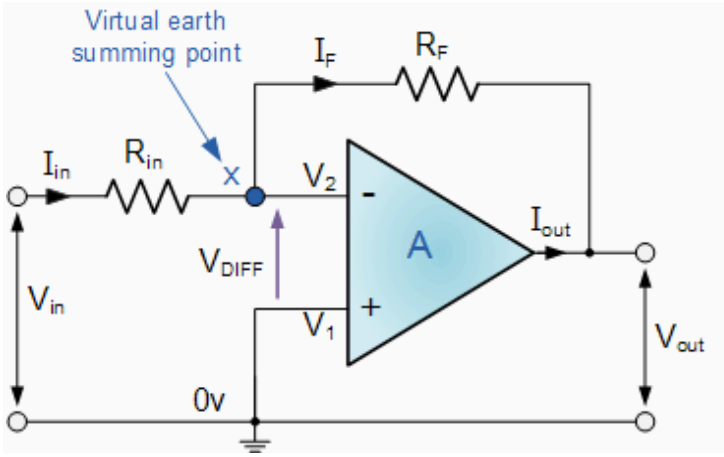
Theory:

The Open Loop Gain, (Av_o) of an ideal operational amplifier can be very high, as much as 1,000,000 (120dB) or more. However, this very high gain is of no real use to us as it makes the amplifier both unstable and hard to control as the smallest of input signals, just a few micro-volts, (μV) would be enough to cause the output voltage to saturate and swing towards one or the other of the voltage supply rails losing complete control. As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external Feedback Resistor called R_f. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero. This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**. A closed-loop amplifier uses negative feedback to accurately control the overall gain but at a cost in the reduction of the amplifiers bandwidth. This negative

feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a *Summing Point*.
We must therefore separate the real input signal from the inverting input by using an Input Resistor, R_{in}. As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below, but the effect of this closed loop feedback circuit results in the voltage potential at the inverting input being equal to that at the non-inverting input producing a *Virtual Earth* summing point because it will be at the same potential as the grounded reference input. In other words, the op-amp becomes a "differential amplifier".

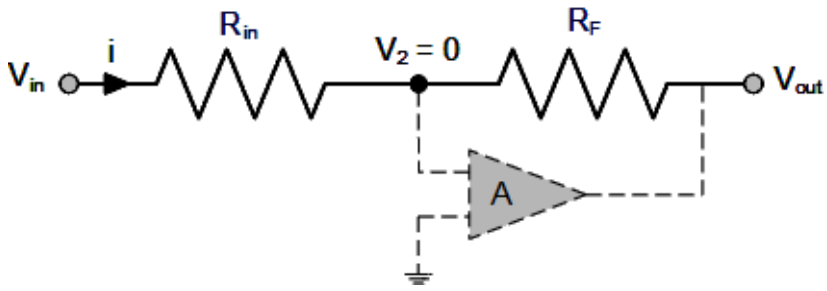
Inverting Amplifier Configuration



In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. For ideal op-amps there are two very important rules to remember about inverting amplifiers, these are: "no current flows into the input terminal" and that "V_1 equals V_2", (in real op-amps both these rules are broken). This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a "Virtual Earth". Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, R_{in} and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about **Inverting Amplifiers** or any operational amplifier for that matter and these are.
1- No Current Flows into the Input Terminal
2- The Differential Input Voltage is Zero as $V_1 = V_2 = 0$ (Virtual Earth)

Then by using these two rules we can derive the equation for calculating the closed-loop gain of an inverting amplifier, using first principles.
Current (i) flows through the resistor network as shown.



$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

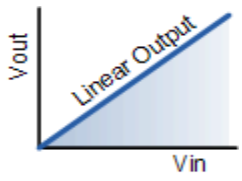
$$\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

$$\text{Gain (Av)} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

and this can be transposed to give V_{out} as:

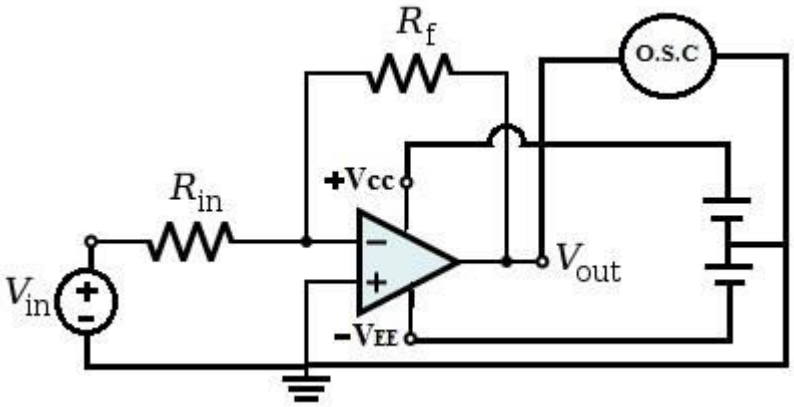
$$Vout = -\frac{Rf}{Rin} \times Vin$$



The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180^o out of phase. This is due to the feedback being negative in value.
The equation for the output voltage V_{out} also shows that the circuit is linear in nature for a fixed amplifier gain as $V_{out} = V_{in}$ x Gain. This property can be very useful for converting a smaller sensor signal to a much larger voltage.
Another useful application of an inverting amplifier is that of a "transresistance amplifier" circuit. A **Transresistance Amplifier** also known as a "transimpedance amplifier", is basically a current-to-voltage converter (Current "in" and Voltage "out"). They can be used in low-power applications to convert a very small current generated by a photo-diode or photo-detecting device etc, into a usable output voltage which is proportional to the input current as shown.

Procedure:

1- Build the circuit, with R_{in}=1KΩ, R_f=10KΩ



3- Check your prediction experimentally for gains of 10 using R_{in}=1KΩ, R_f=10KΩ

Show that the gain of the amplifier is $Av = \frac{Rf}{v_{in}} = \frac{v_{out}}{v_{in}}$

4- Fixed the values of R_{in} and R_f change the frequency of input voltage recorder values of output voltage tabulate your result as below.

f/HZ	v_{in}	v_{out}	Av	Logf/HZ	Av/dB= 20logAv
50					
100					
200					
400					
600					
800					
1000					
2000					
4000					
6000					
8000					
10000					
20000					
40000					
60000					
80000					
100000					
140000					
180000					
200000					

5- Repeat for R_1=1KΩ, R_f=100KΩ
6- Plot graph between log f and A$\boldsymbol{\nu}$ (response frequency) both case in the same graph
7- Measure the bandwidth (the difference between the upper and lower 3 dB points) of the amplifier for each gain. The product of the gain and bandwidth should be constant. Is it?
8- Check the linearity of the amplifier for each gain over its useful frequency range.

Questions for the Lab Report

Why we don't have law cutoff frequency in the operational amplifier?

EXP.NO.15
Physics experiments
3rd stage

Application operation amplifier

Non inverting Amplifier

Object of the experiment:

Study the non inverting amplifier (gain and bandwidth)

Apparatus:

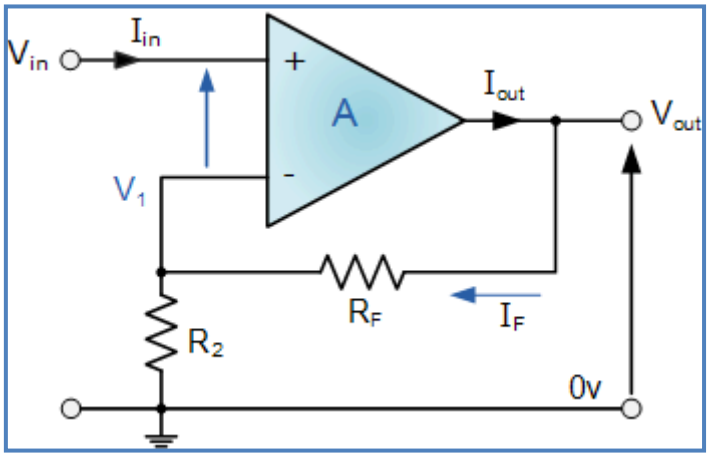
1 DC power supply HY3002-2
1AC power supply
1 operation amplifier LM741
1 plug-in board A4
3 resistance (1KΩ,10KΩ,100KΩ,…..
10 pairs of cables, 50 cm, red/blue

Set up:

Theory:

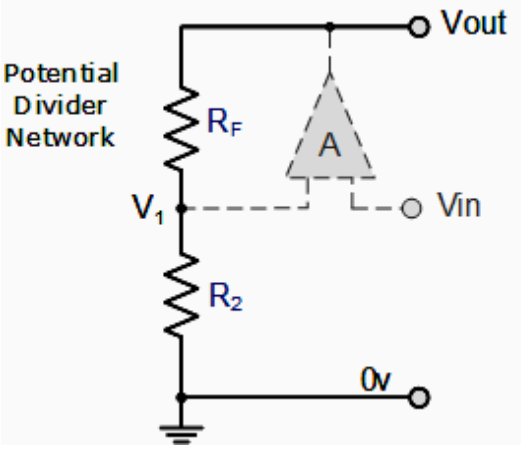
The second basic configuration of an operational amplifier circuit is that of a **Non-inverting Amplifier**. In this configuration, the input voltage signal, (V_{in}) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal. Feedback control of the non-inverting amplifier is achieved by applying a small part of the output voltage signal back to the inverting (-) input terminal via a R_f - R_2 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, R_{in} approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, R_{out} as shown below.

Non-inverting Amplifier Configuration



In the previous Inverting Amplifier tutorial, we said that "no current flows into the input" of the amplifier and that "V_1 equals V_2". This was because the junction of the input and feedback signal (V_1) are at the same potential in other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, R_f and R_2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R_2 and R_f as shown below.

Equivalent Potential Divider Network



Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain (A_v) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

Ideal Summing Point: $V_1 = V_{IN}$

Voltage Gain, $A_{(V)}$ is equal to: $\frac{V_{OUT}}{V_{IN}}$

Then, $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$

Transpose to give: $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$

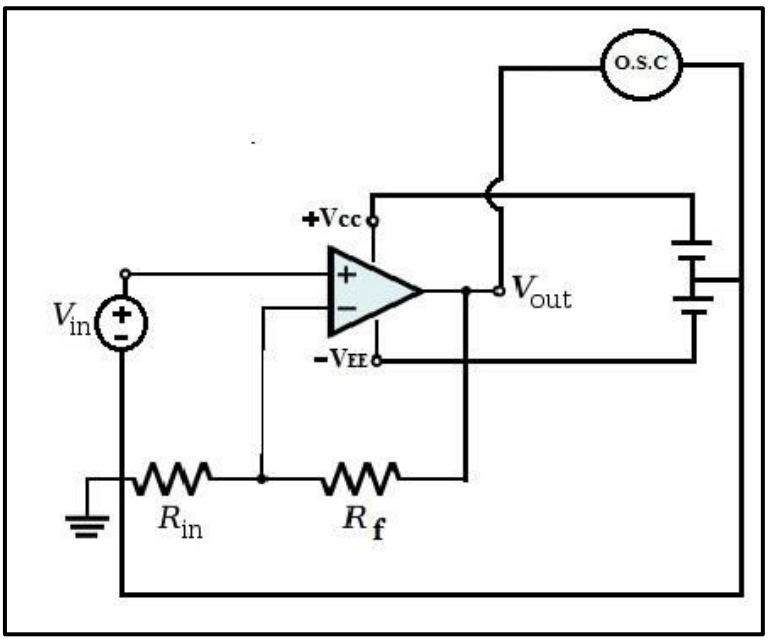
Then the closed loop voltage gain of a **Non-inverting Amplifier** is given as:

$$A_{(v)} = 1 + \frac{R_F}{R_2}$$

We can see from the equation above, that the overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio of the values of R_f and R_2. If the value of the feedback resistor R_f is zero, the gain of the amplifier will be exactly equal to one (unity). If resistor R_2 is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, (A_o).

Procedure:

1- Build the circuit, and check your prediction experimentally for gains of 11 by using R_{in}=1KΩ, R_f=10KΩ



2- . Show that the gain of the amplifier is $Av = \frac{Rf}{Rin} + 1 = \frac{v_{out}}{v_{in}}$

3- Fixed the values of R_{in} and R_f change the frequency of input voltage recorder values of output voltage tabulate your result as below.

R_1=1KΩ, R_2=10KΩ

f/HZ	v_{in} /V	v_{out}/V	Av	Logf/HZ	Av/dB= 20logAv
50					
100					
200					
400					
600					
800					
1000					
2000					
4000					
6000					
8000					
10000					

20000					
40000					
60000					
80000					
100000					
140000					
180000					
200000					

Repeat for R_1=1KΩ, R_f=100KΩ

3- Measure the bandwidth (the difference between the upper and lower 3 dB points) of the amplifier for each gain. The product of the gain and bandwidth should be constant. Is it?
4- Check the linearity of the amplifier for each gain over its useful frequency range.

Questions for the Lab Report

Define open loop cutoff frequency how can we find it graphically?

EXP.NO.16
Physics experiments
3rd stage

Application operation amplifier

Differentiator Amplifier

Object of the experiment:

Study Differentiator Amplifier Circuit

Apparatus:

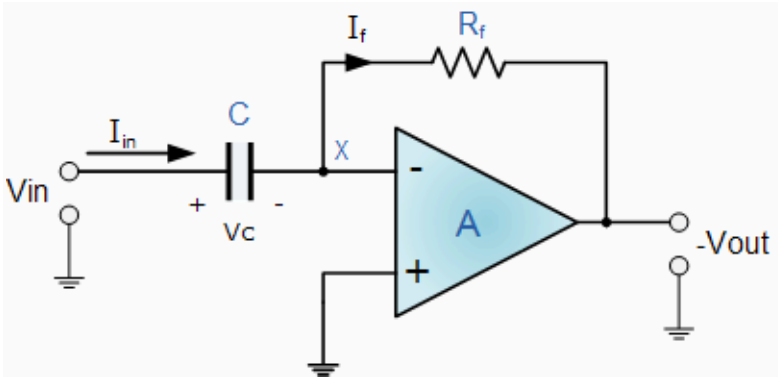
1 DC power supply HY3002-2
1TRIO audio generator AG202A
1 operation amplifier LM741
1 plug-in board A4
2 resistance (1KΩ,10KΩ,100KΩ,…..
1 capacitor 0.1µf
10 pairs of cables, 50 cm, red/blue

Set up:

Theory:

The basic Differentiator Amplifier circuit is the exact opposite to that of the Integrator operational amplifier circuit that we saw in the previous tutorial. Here, the position of the capacitor and resistor have been reversed and now the reactance, X_c is connected to the input terminal of the inverting amplifier while the resistor, R_f forms the negative feedback element across the operational amplifier as normal. This circuit performs the mathematical operation of Differentiation that is it "produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape. As with the integrator circuit, we have a resistor and capacitor forming an R_C Network across the operational amplifier and the reactance (X_c) of the capacitor plays a major role in the performance of a Differentiator Amplifier.

Differentiator Amplifier Circuit



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal. At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R_f/X_c) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies a differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R_f.

Ok, some math's to explain what's going on! Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \quad \text{and} \quad I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the Differentiator Amplifier is given as:

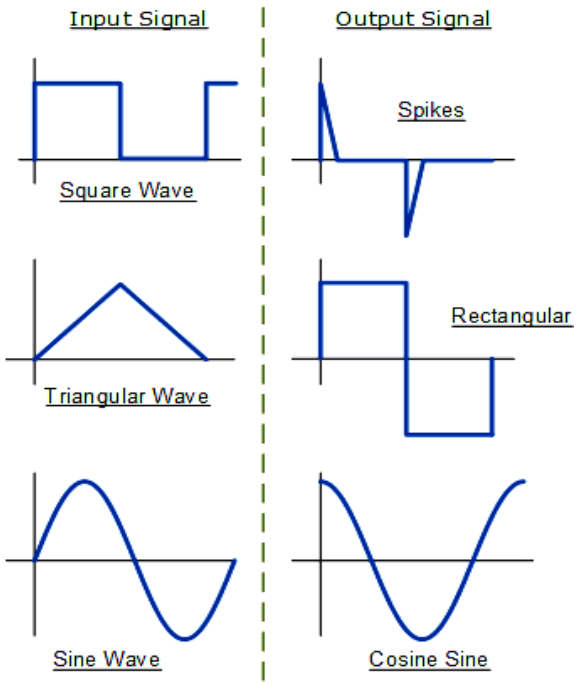
$$V_{OUT} = -R_F C \frac{dV_{IN}}{dt}$$

Therefore, the output voltage V_{out} is a constant $-R_f.C$ times the derivative of the input voltage V_{in} with respect to time. The minus sign indicates a 180^o phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

One final point to mention, the Differentiator Amplifier circuit in its basic form has two main disadvantages compared to the previous integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required

Differentiator Waveforms

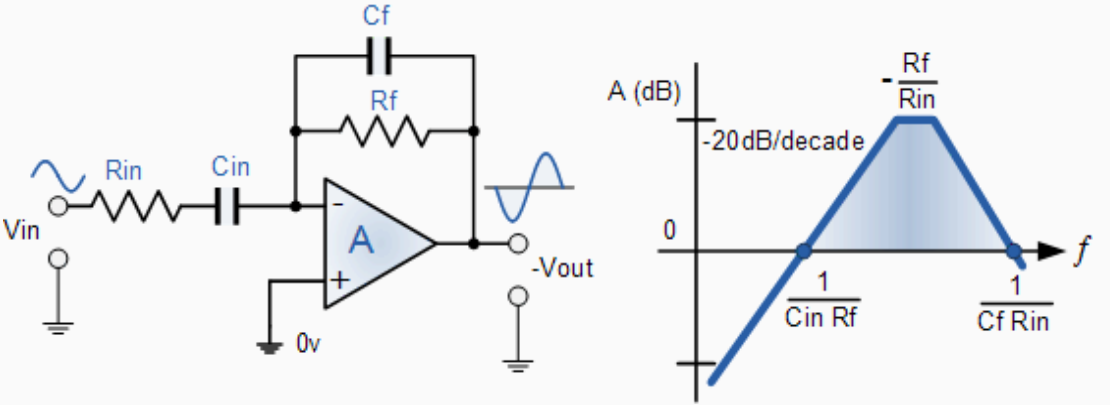
If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependent upon the RC time constant of the Resistor/Capacitor combination.



Improved Differentiator Amplifier

The basic single resistor and single capacitor differentiator circuit is not widely used to reform the mathematical function of Differentiation because of the two inherent faults mentioned above, Instability and Noise. So in order to reduce the overall closed-loop gain of the circuit at high frequencies, an extra resistor, Rin is added to the input as shown below.

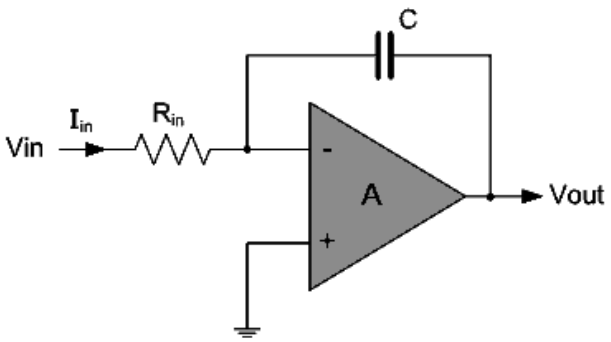
Improved Differentiator Amplifier Circuit



Adding the input resistor Rin limits the differentiators increase in gain at a ratio of R_f/R_{in}. The circuit now acts like a differentiator amplifier at low frequencies and an amplifier with resistive feedback at high frequencies giving much better noise rejection. Additional attenuation of higher frequencies is accomplished by connecting a capacitor C_1 in parallel with the differentiator feedback resistor, R_f. This then forms the basis of an Active High Pass Filter as we have seen before in the filters section

Procedure:

1- Build the circuit, with R_{in}=1KΩ, C=0.1µf and use square and sinusoidal wave forms to test the predicted behavior. Also place a 100KΩ resistor in series with the capacitor. This resistor drains charge to avoid saturation due to very low frequency or DC signals.



2- check your prediction experimentally for the condition of integrator RC << $\mathcal{T}$ where $\mathcal{T} = \frac{1}{f}$

3- Draw the input and output wave from OSC.

4- Show that the relation between input and output voltage is :

$$v_o = -RC\frac{dv_{in}}{dt}$$

5- Change the value of R or C and draw output wave and discuses your result?

6- Use sinusoidal wave forms:
What waveform do we expect at the differentiator's output?
If $V_S = A \cdot \sin(\omega \cdot t)$, then $dV_S / dt = \omega \cdot A \cdot \cos(\omega \cdot t)$. Extending this equation to the circuit, we get

$$v_o = -C_1 \cdot R_2 \frac{dv_s}{dt}$$

$$= -C1 \cdot R2 \cdot \omega \cdot A \cdot \cos(\omega \cdot t)$$

Questions for the Lab Report

What is the role of R_{in} and R_f?
Give some applications of the differentiator?

EXP.NO.17
Physics experiments
3rd stage

Application operation amplifier

The Integrator Amplifier

Object of the experiment:

Study the application of amplifier (integrator)

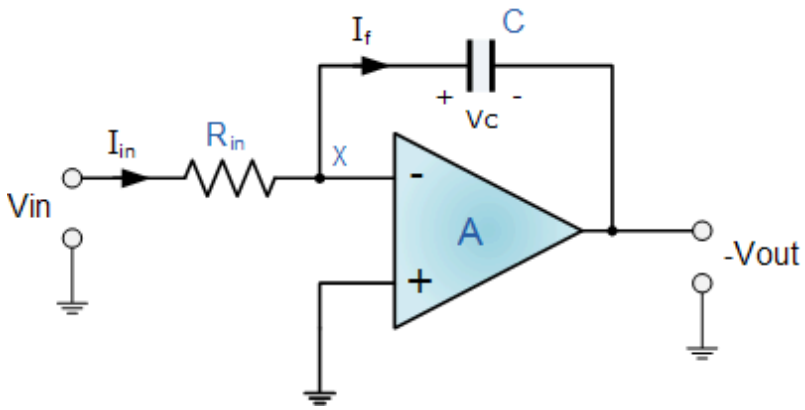
Apparatus:

1 DC power supply HY3002-2
1AC power supply
1 operation amplifier LM741
1 plug-in board A4
2 resistance (1KΩ,10KΩ,100KΩ,…..
2 capacitor (0.1μf,0.01μf
10 pairs of cables, 50 cm, red/blue

Set up:

Theory:

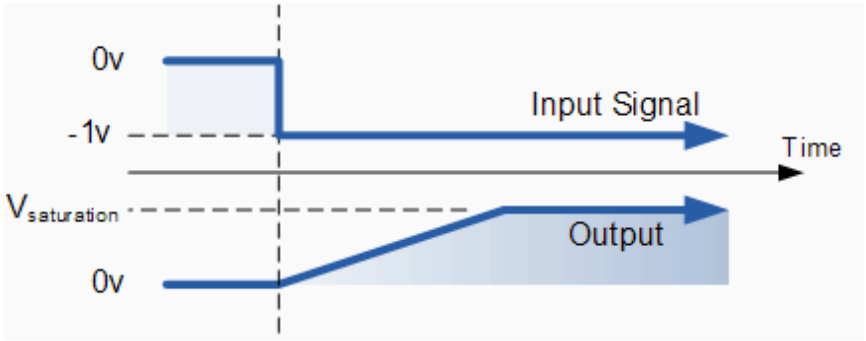
In the previous tutorials we have seen circuits which show how an operational amplifier can be used as part of a positive or negative feedback amplifier or as an adder or subtract or type circuit using just pure resistances in both the input and the feedback loop. But what if we were to change the purely resistive (R_f) feedback element of an inverting amplifier to that of a frequency dependant impedance, (Z) type complex element, such as a Capacitor, C. What would be the effect on the output voltage? By replacing this feedback resistance with a capacitor we now have an RC Network across the operational amplifier as shown below.



As its name implies, the **Integrator Amplifier** is an operational amplifier circuit that performs the mathematical operation of **Integration**, that is we can cause the output to respond to changes in the input voltage over time. The integrator amplifier acts like a storage element that "*produces a*

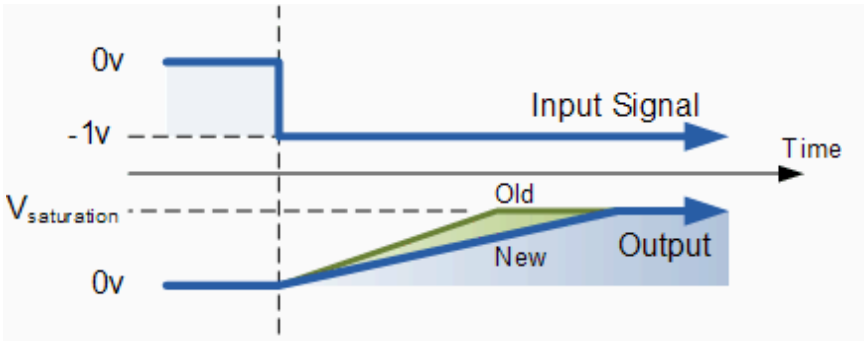
voltage output which is proportional to the integral of its input voltage with respect to time". In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a voltage, V_{in} is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit (voltage follower circuit) giving an overall gain of less than one. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the feedback capacitor C begins to charge up, its reactance Xc decreases this results in the ratio of Xc/R_{in} increasing producing an output voltage that continues to increase until the capacitor is fully charged. At this point the capacitor acts as an open circuit, blocking anymore flow of DC current. The ratio of feedback capacitor to input resistor (X_c/R_{in}) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).



The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, "RC time constant". By changing this RC time constant value, either by changing the value of the Capacitor, C or

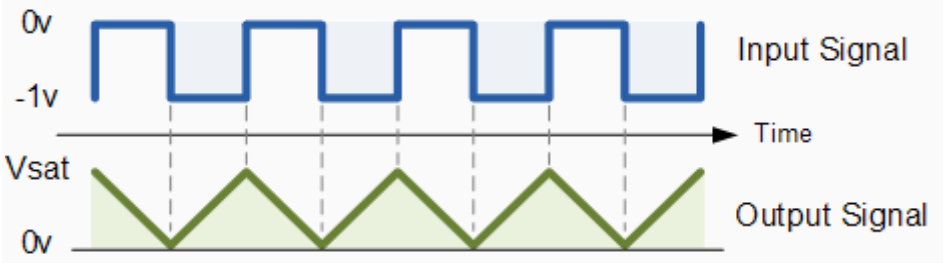
the Resistor, R, the time in which it takes the output voltage to reach saturation can also be changed for example.



If we apply a constantly changing input signal such as a square wave to the input of an **Integrator Amplifier** then the capacitor will charge and discharge in response to changes in the input signal.

This results in the output signal being that of a sawtooth waveform whose frequency is dependent upon the RC time constant of the resistor/capacitor combination. This type of circuit is also known as a Ramp Generator and the transfer function is given below.

Ramp Generator



We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout therefore: -Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \qquad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, $X = 0$, the input current I_{in} flowing through the input resistor, R_{in} is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 0$$

From which we derive an ideal voltage output for the **Integrator Amplifier** as:

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC}V_{in}$$

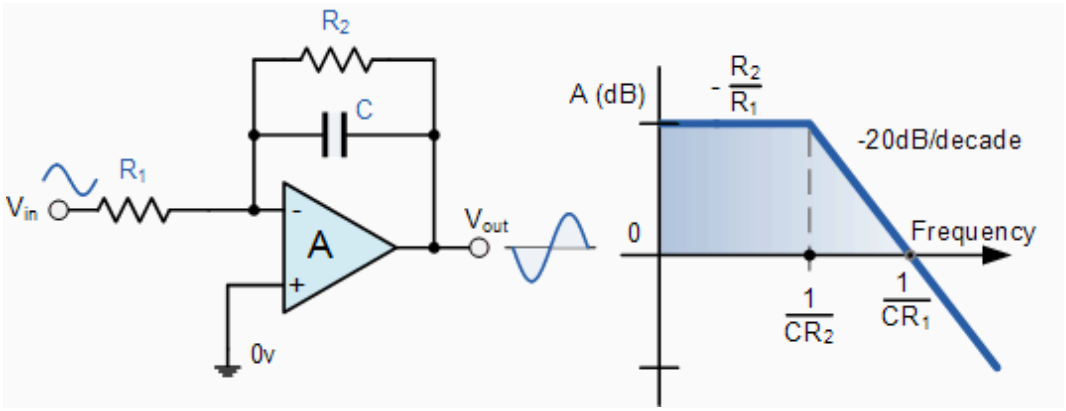
Where $j\omega = 2\pi f$ and the output voltage V_{out} is a constant $1/RC$ times the integral of the input voltage V_{in} with respect to time. The minus sign (-) indicates a 180^o phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

The AC or Continuous Integrator

If we changed the above square wave input signal to that of a sine wave of varying frequency the **Integrator Amplifier** performs less like an integrator and begins to behave more like an active "Low Pass Filter", passing low frequency signals while attenuating the high frequencies. At 0Hz or DC, the capacitor acts like an open circuit blocking any feedback voltage resulting in very little negative feedback from the output back to the input of the amplifier. Then with just the feedback capacitor, C, the amplifier effectively is connected as a normal open-loop amplifier which has very high open-loop gain resulting in the output voltage saturating.

This circuit connects a high value resistance in parallel with a continuously charging and discharging capacitor. The addition of this feedback resistor, R_2 across the capacitor, C gives the circuit the characteristics of an inverting amplifier with finite closed-loop gain of R_2/R_1 at very low frequencies while acting as an integrator at higher frequencies has the capacitor shorts out the feedback resistor, R_2.

The AC Integrator with DC Gain Control



Unlike the DC integrator above whose output voltage at any instant will be the integral of a waveform so that when the input is a square wave, the output waveform will be triangular. For an AC integrator, a sinusoidal input waveform will produce another sine wave as its output which will be 90° out-of-phase with the input producing a cosine wave.

Further more, when the input is triangular, the output waveform is also sinusoidal. This then forms the basis of a **Active Low Pass Filter** as seen before in the filters section tutorials with a corner frequency given as.

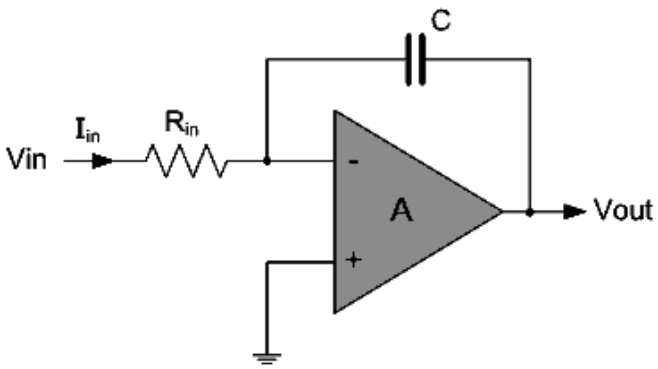
$$\text{D.C. Voltage Gain, } (Av_0) = -\frac{R_2}{R_1}$$

$$\text{A.C. Voltage Gain, } (Av) = -\frac{R_2}{R_1} \times \frac{1}{(1+2\pi f C R_2)}$$

$$\text{Corner Frequency, } (f_0) = \frac{1}{2\pi C R_2}$$

Procedure:

1- Build the circuit with Rin=1 KΩ, C=0.1µf and use square and sinusoidal wave forms to test the predicted behavior. Also place a 100MΩ resistor in parallel with the capacitor. This resistor drains charge to avoid saturation due to very low frequency or DC signals.



2- and check your prediction experimentally for the condition of integrator $RC >> T$ where $\mathcal{T} = \frac{1}{\text{f}}$
3- Draw the input and output wave from OSC.
4- Show that the relation between input and output voltage is :

$$v_o = -\frac{1}{RC}\int v_{in}\, dt$$

5- Change the value of Rin and draw output wave and discuses your result?

Questions for the Lab Report

What is the role of R_2?
Give some applications of integrator?