[JER] Article Review Request

1 message

Mrs.Jisha Sara via Open Journal Systems <jer@ku.edu.kw>
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Sun, Nov 13, 2022 at 10:05 AM

Prof Muhammed Abdulbaki Ibrahim:

This regards the manuscript "A differential block and NCG cell based four stage CMOS amplifier," which is under consideration by Journal of Engineering Research.

Following the review of the previous version of the manuscript, the authors have now submitted a revised version of their paper. We would appreciate it if you could help evaluate it.

Please log into the journal web site by 2022-11-19 to indicate whether you will undertake the review or not, as well as to access the submission and to record your review and recommendation.

The review itself is due 2022-12-17.

Submission URL: https://kuwaitjournals.org/jer/index.php/JER/reviewer/submission?submissionId=18023&reviewId=41689&key=HH5v8FSA

Thank you for considering this request.

Mrs.Jisha Sara
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"A differential block and NCG cell based four stage CMOS amplifier"

Abstract

In this paper, a four stage CMOS operational amplifier is proposed to drive a large capacitive load of 500 pF. The designed operational amplifier shows high stability besides meeting intended specifications like high gain, good swing etc. It is already known that the number of high impedance nodes increases as number of stages in amplifier increases so design of frequency compensation network for a four stage amplifier has been a quite challenging work. The designed compensation network exploited in this work is unique and is the combination of negative capacitance generator (NCG) cell and a differential block along with a compensation capacitor. The NCG cell's incorporation has lowered preceding stage's parasitic capacitance resulting in to improvement in GBW significantly and use of differential block in feed forward path has resulted into reduction of compensation capacitor's value. The substantiality of the proposed design is verified with help of a number of simulations and theoretical analysis. Simulation results are found in good agreement with the theoretical description. The implemented amplifier shows 156.54 dB, 86.68º and 35.82 MHz as DC gain, phase margin (PM) and Gain Bandwidth (GBW) respectively. The Large signal step response reveals that the

simulated four stage CMOS amplifier's step response settles within 475 ns with 5% settling error. All simulations have been carried out using 0.18 µm CMOS technology parameters in cadence virtuoso simulator. The supply voltage is set to 1.8 V while power consumption is 1.67 mW.