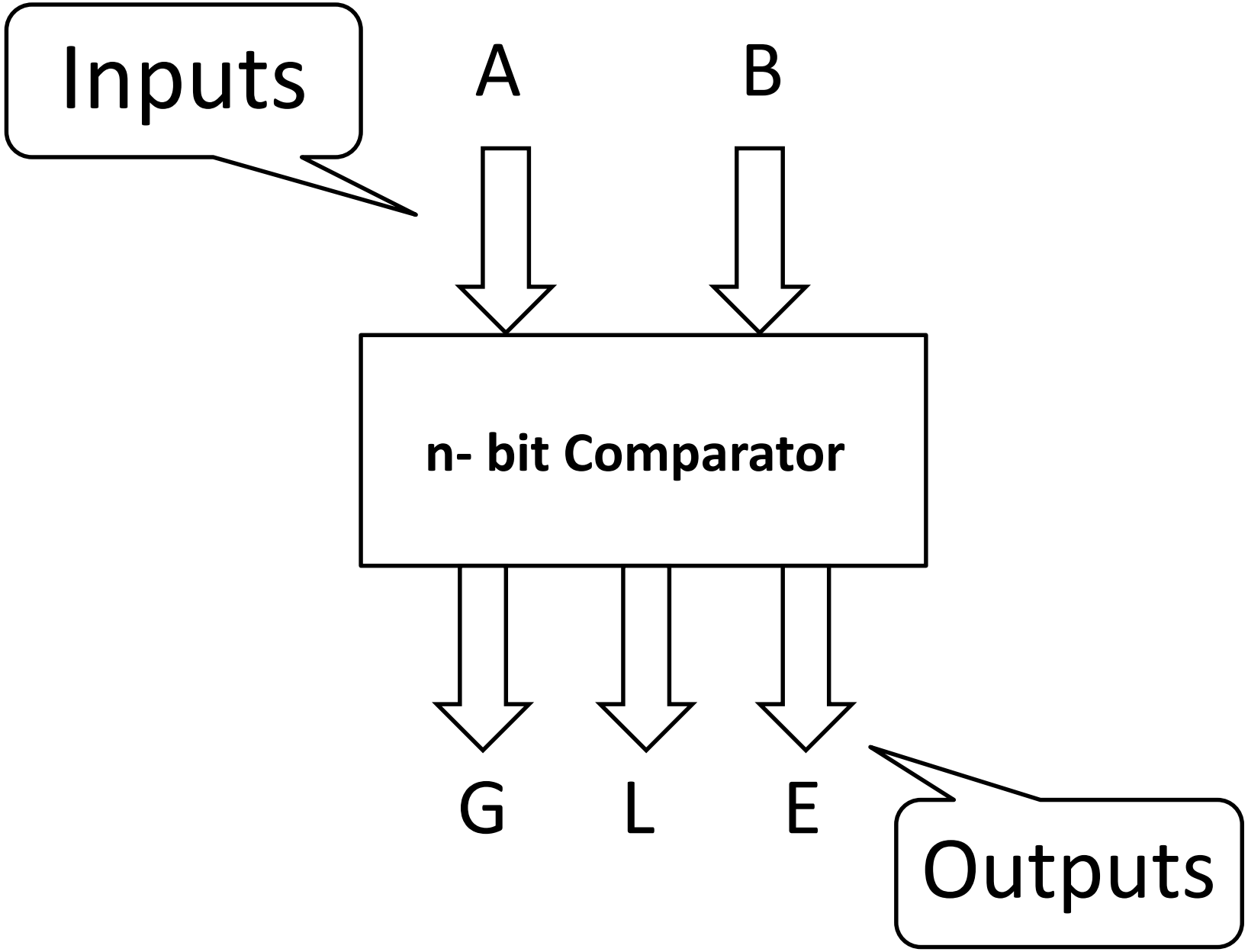
Digital Magnitude Comparator

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers .an n-bit comparator receives two n-bit numbers A and B as inputs and the outputs are:

- A > B (G)
- A < B (L)
- A = B (E)


Inputs
A
B
n- bit Comparator
G
L
E
Outputs

1 bit Comparator

DEC.	A	B	G	L	E
0	0	0	0	0	1
1	1	0	1	0	0
2	0	1	0	1	0
3	1	1	0	0	1

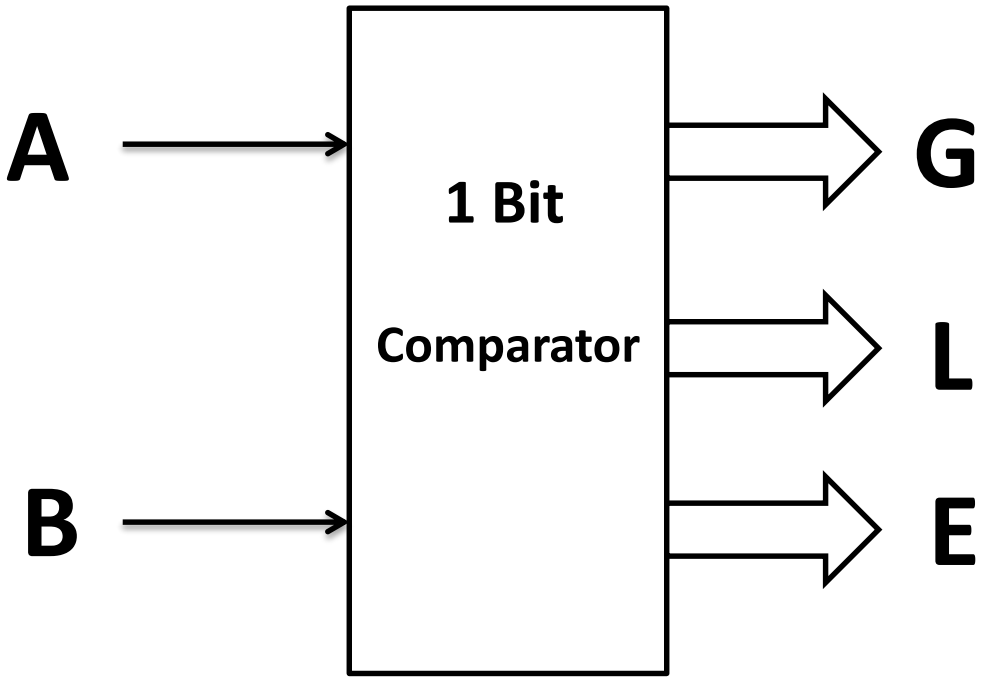
1 bit Comparator

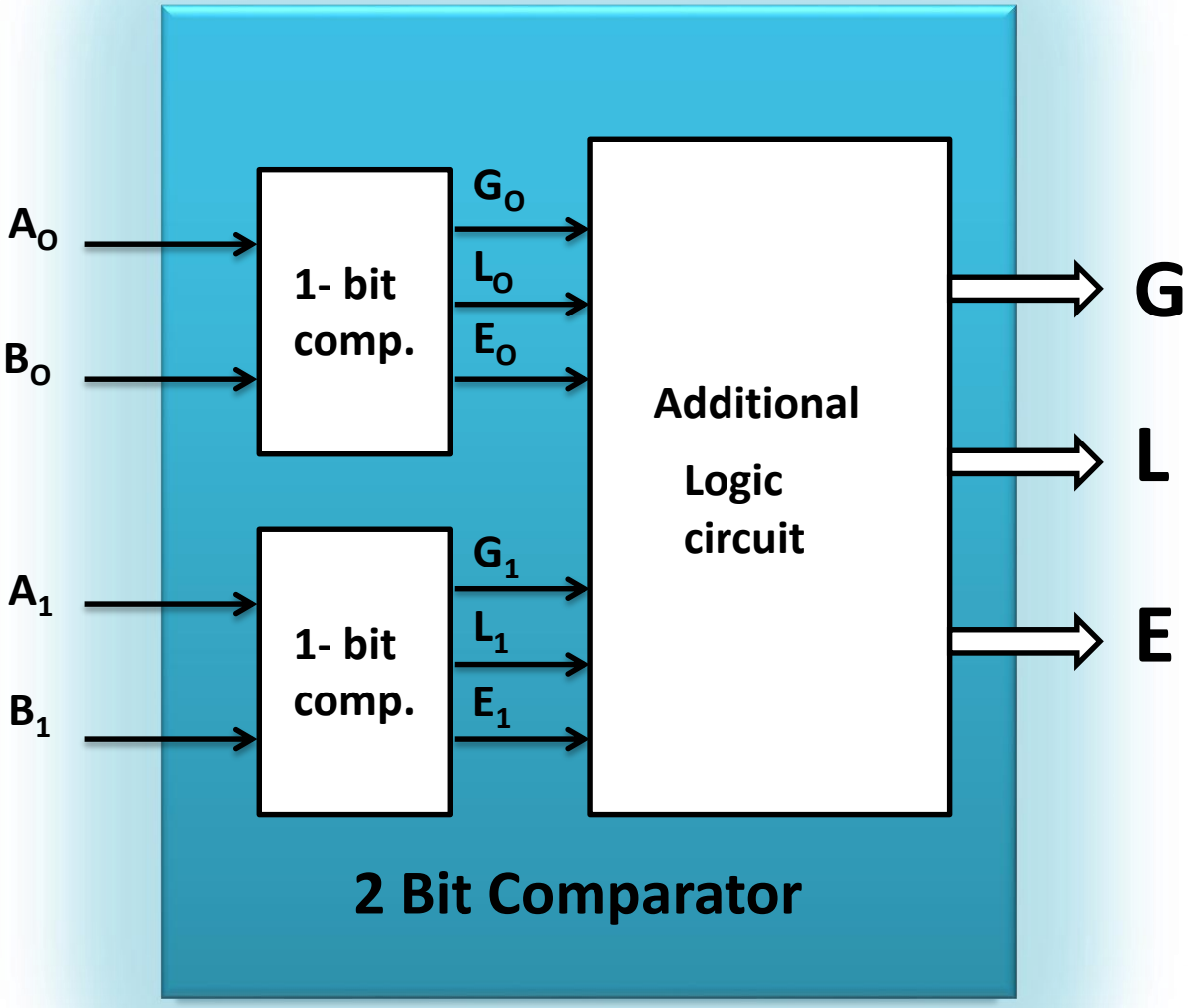
$$G = A\overline{B}$$

$$L = \overline{A}B$$

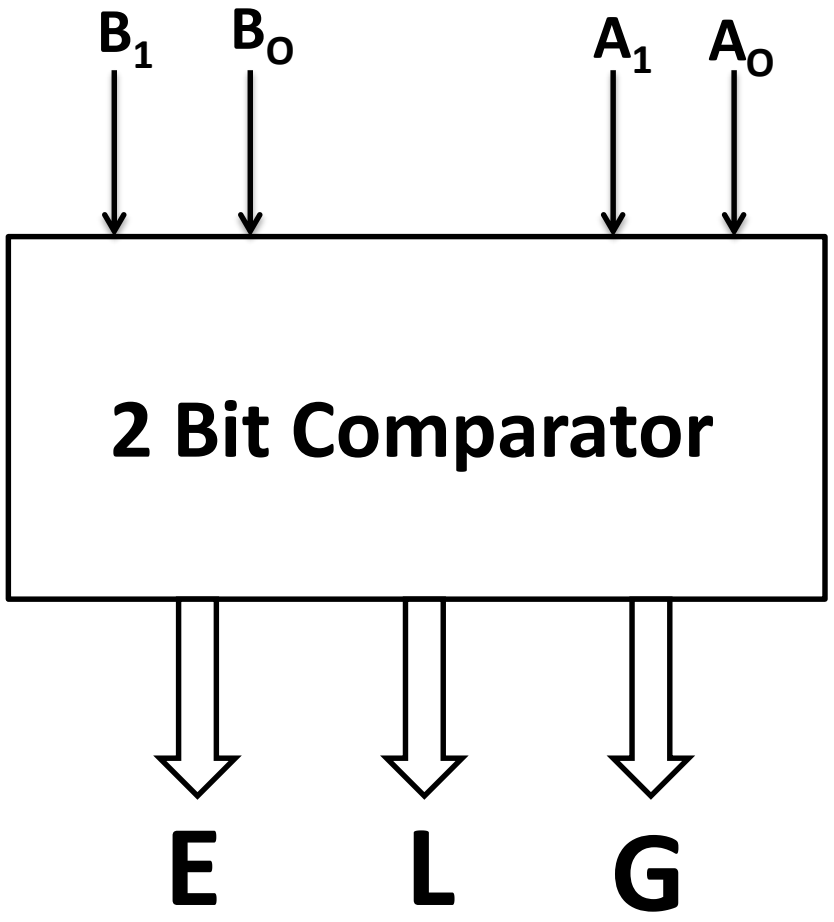
$$E = \overline{A}\,\overline{B} + AB$$

1 Bit Comparator




A_O
B_O
1- bit comp.
G_O
L_O
E_O
A_1
B_1
1- bit comp.
G_1
L_1
E_1
Additional Logic circuit
G
L
E
2 Bit Comparator

2 Bit Comparator



If $A_1 < B_1$ or $A_1 = B_1$ And $A_O < B_O$

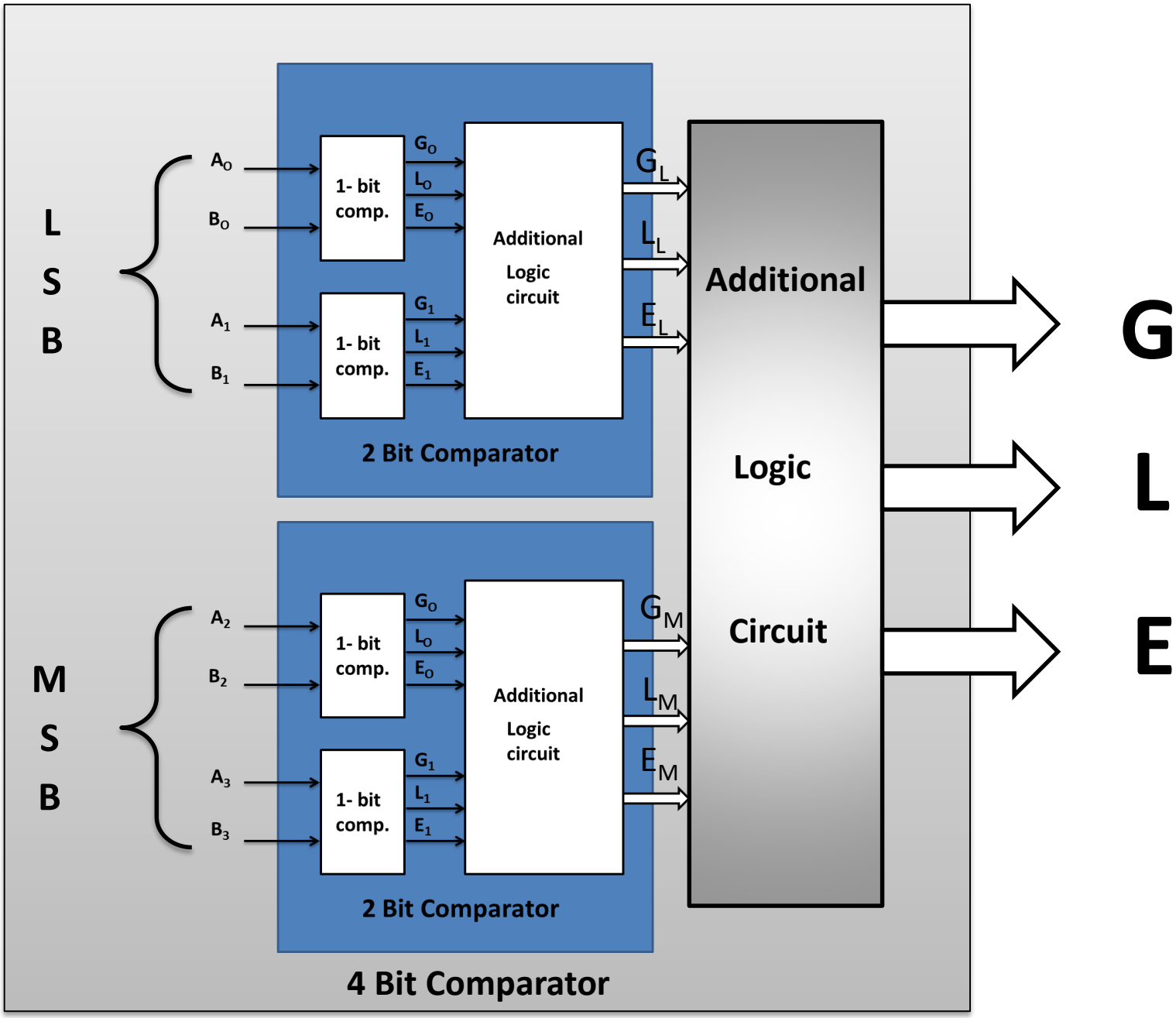
$$G = G_1 + E_1 . G_O$$

If $A_1 > B_1$ or $A_1 = B_1$ And $A_O > B_O$

$$L = L_1 + E_1 . L_O$$

If $A_1 = B_1$ and $A_O = B_O$

$$E = E_1 . E_0$$

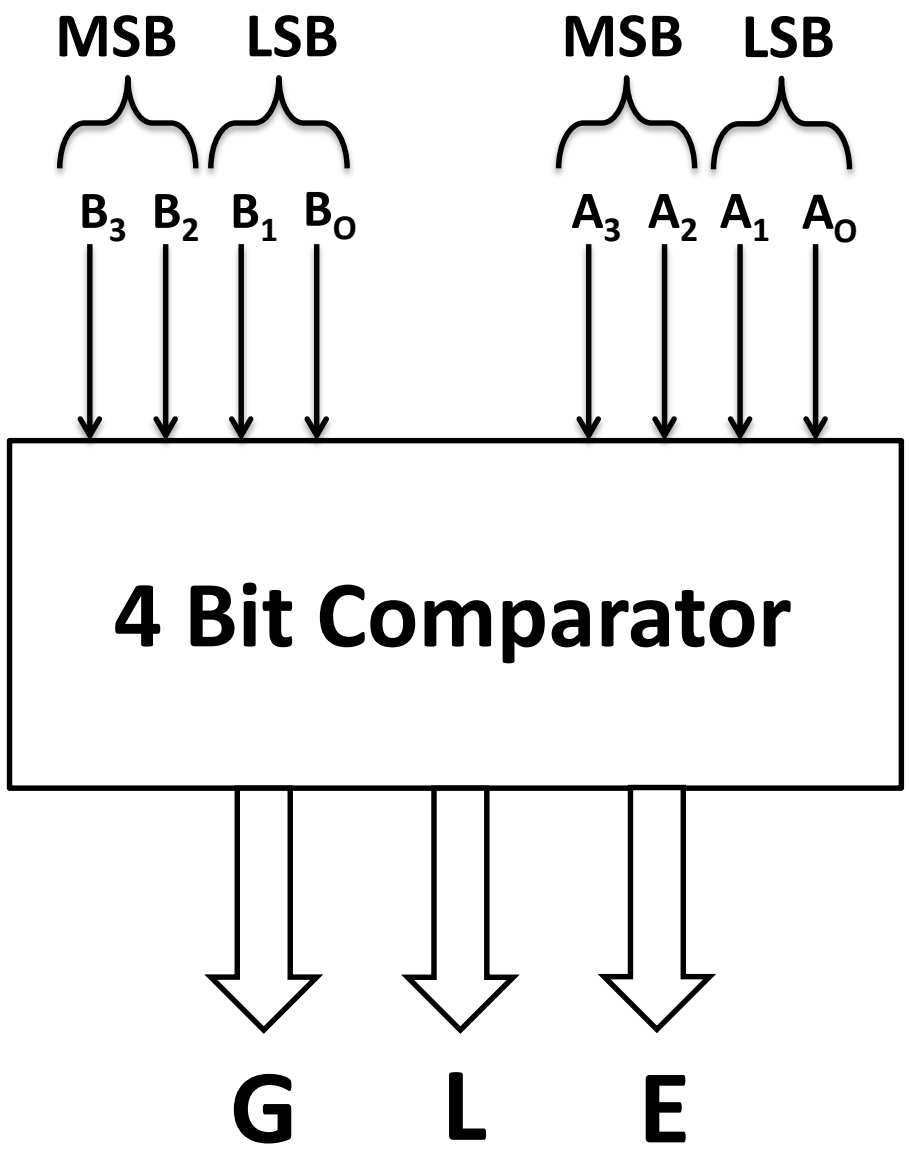

LSB
MSB
A_0
B_0
A_1
B_1
A_2
B_2
A_3
B_3
1- bit comp.
1- bit comp.
1- bit comp.
1- bit comp.
G_0
L_0
E_0
G_1
L_1
E_1
Additional Logic circuit
Additional Logic circuit
2 Bit Comparator
2 Bit Comparator
G_L
L_L
E_L
G_M
L_M
E_M
Additional Logic Circuit
G
L
E
4 Bit Comparator

4 Bit Comparator

$$G = G_M + E_M \cdot G_L$$

$$L = L_M + E_M \cdot L_L$$

$$E = E_M \cdot E_L$$


MSB
LSB
MSB
LSB
B_3 B_2 B_1 B_O
A_3 A_2 A_1 A_O
4 Bit Comparator
G
L
E