



*Salahaddin University-Hawler
College of Engineering
Software department*



Sample of Questions

Computer Architecture

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Level of Course: Undergraduate Degree

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1. Solve the following Equation using One -address format $Y=(A*B)+(C/D)-B$
2. Transfer the following code from High level language to low level language;


```

      { int x=3,y=8;
        If (x>y)      x=x+y;
        Else if (x<y) x=x-y;
        Else          x=y-x;
      }
      
```
3. How the structure of the computer to be dividing to levels (explain briefly by steps) ?
4. All the operating system types were applications while not every application was an operating system (clarify this statement)?
5. Draw a block diagram that performs the CPU Function operation?
6. What are the difference between the job done by PC as a compared with MAR?
7. Example: let the PC=100 (which is the address of the first instruction), and the partial list of code to be ;

00001 :- load AC from memory,	AC ← Memory
00010 :-copy AC to B register	B ← AC
00101:- Add AC to memory contains	AC ← AC + Memory
00111: copy AC to C register	C ← AC
01111:-END	

Let IR size =16 bit, and the memory contains as follows:

100	01740
101	0 5741
102	02741
103	0F000
.	.
.	.
740	00044
741	00002

- a- Trace on the configuration above and find any changing to be happen on any register or memory location rather than end ?
 - b- How many instructions executed?
 - c- Write the sub program that implement using the configuration above?
8. Explain LOAD and STOR and clarify any similar instructions used with the stack?
 9. Check the branching of the following instruction and find PC values?

203 BRZ 211

10. Trace on the following assembly program and answer the questions below it;

```
MOV R2, 200h           ; initialize R2
MOV R0, 6              ; initialize counter R0
MOV R1, 0              ; initialize R1
back: ADD R1, [R2]
INC R2
DEC R0
BRNZ back              ; branching if no zero result of
R0
END
```

- a- What was the operation need to implement using this program?
 - b- Are there are any loop in it if so how many time the looping statements executed?
 - c- Which type of addressing to memory used and by which register?
11. Write an assembly program to find the summation of 10 memory location begin by [200] and save the result in the stack segment?
12. Write an assembly program to swap three register values without using any other temporary register?
13. What are the operation performed by the following sub program :

```
PUSH A
PUSHB
POP A
POP B
```

14. Check on this program (let all the registers were 8-bit size):

```
MOV R1, 4
MOV R2, 100
MOV R3, 2
MOV [R2], R1
SHL [R2], R3           ;shift left
INC [R2]               ;increment by one
LDA R2
```

- a- Specify the operation performed by each instruction (i.e.) Registers, and memory location changes.
- b- What are the addressing mode of each instruction above.

15- Trace on this program and answer the branches below it:

```

MOV R1,4
MOV R2,100
MOV R3,2
MOV [R2],R1
SHR [R2],R3
INC [R2]          ; increment by one
LDA R2
    
```

- a- Specify the operation performed by each instructions (i.e.) Registers and memory location changes.
- b- What are the addressing modes of each instruction above

16- Write an assembly program in "one address format" to implement the following equation:

$$y = \frac{1}{(A - B * C)^2} + B$$

- 17- Transfer the equation above from infix notation to postfix notation
- 18- Implement the same equation by Stack Based programming and clarifies its difference with the program in branch (A)?
- 19- Let $A=(10110111)_2$, and $B=(00001101)_2$, Find the result as follows:

	Operation	Result=?	Sign Flag=?	Negative or Possative
1	(-A) + (+B)			
2	(+A) - (+B)			
3	(+A) - (-B)			
4	(-A) + (-B)			

20- Transfer this sub program to low level language to perform the same job:

```

int x=5;
switch(x)
{
Case 1: x=x+1;
break;
Case 2: x=x-1;
break;
Default: x=0;
}
    
```

21- Let the PC=10A, R1=300h (which is the address of the first instruction), and the partial list of code to be;

0001 :-load R1 from memory,
 0010 :- load AC from memory,
 0011 :-Store AC to memory,
 0100 :- SUB AC to memory contains.
 0101 :-end of program
 0110:- ADD AC to memory.

Let IR, AC, R1 registers size =16 bit, and the memory contains as follows
 Applying micro operation to each instruction in order to :

10A	2200
10B	4201
10C	3201
10D	1201
10E	5000
.	.
200	010F
201	001E
202	0000

- a) Specify the value of registers (AC, IR, and R1), with updated memory location.
- b) Find how many instructions to be executed rather than reach to end.

- 22- What is the general relationship among access time, memory cost, and capacity?
- 23- What are the differences among direct mapping, associative mapping, and set associative mapping?
- 24- A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses?
- 25- A two-way set-associative cache has lines of 16 bytes and a total size of 8 k bytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.
- 26- suppose that a computer system have two level of memory unit L1 is the cache memory have access time $0.02\mu s$; and L2 is the main memory of access time $0.2\mu s$, is the percentage of data occurrence in L1 is 15%, find the average access time ? Is the cache benefit in this case explaining your answer briefly?
- 27- Suppose a computer system operate in set associative mode consist of cache memory capacity 512 Kbyte, 256K lines, and 64 K is the number of set in the cache memory, if the tag field size is 4 bit; evaluate :
- a) Number of line in each set (set size)?
 - b) Memory organization address field?
 - c) Size of main memory?
 - d) Number of block in main memory?

28- : If there are 16 K line in the cache memory, evaluate the line address of the following main memory address field in a direct addressing mapping, where the word field consist of 2 bit:

- a) FF339C (H)
- b) E2AA31 (H)
- c) 001110 (H)
- d) 123456 (H)

29- Trace on this program and answer the branches below it:

(Let all the registers were 8-bit size)

```

MOV R1,4
MOV R2,100
MOV R3,2
MOV [R2],R1
SHR [R2],R3
INC [R2] ; increment by one
LDA R2
    
```

c- Specify the operation performed by each instructions (i.e.) Registers and memory location changes.
(14 mark)

30- What are the addressing modes of each instruction in the question 29?

31- Write an assembly program in "one address format" to implement the following equation:

$$y = \frac{1}{(A - B * C)^2} + B$$

32- Transfer the equation above from infix notation to postfix notation

33- Implement the same equation by Stack Based programming and clarifies its difference with the program in branch (A)?

34- Let A=(10110111)₂ , and B=(00001101)₂ , Find the result as follows:

	Operation	Result=?	Sign Flag=?	Negative or Possative
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35- Transfer this sub program to low level language to perform the same job:

```

int x=5;
switch(x)
{
Case 1: x=x+1;
break;
Case 2: x=x-1;
break;
Default: x=0;
}
    
```

36- Let the PC=10A, R1=300h (which is the address of the first instruction), and the partial list of code to be;

0001 :-load R1 from memory,
 0010 :- load AC from memory,
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 0100 :- SUB AC to memory contains.
 0101 :-end of program
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Let IR, AC, R1 registers size =16 bit, and the memory contains as follows
 Applying micro operation to each instruction in order to :

2200	10A
4201	10B
3201	10C
1201	10D
5000	10E
.	.
010F	200
001E	201
0000	202

- c) Specify the value of registers (AC, IR, and R1), with updated memory location.
- d) Find how many instructions to be executed rather than reach to end.

37- Using Multiplication Algorithm find (1011011) * (1001)

38- Is there any difference for using Q,M Registers in question (37) for each value; if so which one is the best?

39- Using Division Algorithm find (1011011) / (1001)

40- Is there any difference for using Q,M Registers in question (39) for each value; if so which one is the best?

41- Draw a block diagram of designing unsigned binary Multiplication?

42- Draw the flowchart of unsigned binary Division?

43- Draw the flowchart of unsigned binary Multiplication?

44- Design an 8- bit ALU capable to perform the following 8 micro operations:

{ $F = A+B+C$, $F=B-C$, $F=C-A$, $F = A.B'$, $F = C'$, $F=(B+C)'$, $F = A.B$, $F=(B'.C')$ }

45- If you have 3- logical micro operations and 7- Arithmetic micro operations which type of MUX used to design your ALU?

46- Design an ALU that have three input operands A, B, and C register, and each can hold 8-bit data, and the following micro operation can be performed in it:

- 1) $F=A+B$
- 2) $F=B-A$
- 3) $F=1-C$
- 4) $F=B-1$
- 5) $F=A+B+C$
- 6) $F=A.C'$

47- Let a system of the main memory size was 4G byte, and partitioned to blocks of size 16 word, which have been mapped using direct technique to a cache memory of size 1 M byte, find :

- the main memory address field,?
- Number of block in main memory?

48- Let the average access time were $0.02\mu\text{sec}$, of a system can be connect to two memory level L1 (cache memory) of access time $0.01\ \mu\text{sec}$, and the access time to L2(main memory) was $0.1\ \mu\text{sec}$. Find:

- Percentage of pre processed data in L1 , L2
- Is the cache benefit in this case.

49- State the difference between each of the following briefly:

1. Cache hit and Cache miss
2. Magnetic disk and main memory

50- Design the specific block diagram of shift 4- bit register A, applying the following cases:

1. Parallel input
2. Shift left (A) one time
3. Shift left (A) two time
4. Shift right (A) one time
5. Shift right (A) two time

51- Transfer the following expression from infix notation to Reverse polish notation:

$$Y = A/B/C - D^2 * F$$

, then use the stack procedure to check on your result?

52- implement this program and then answer the branches below

```
100  MOV Y, 40h
102  MOV X, F2h
104  SHR X, 1h
106  SUB X, Y
108  JGT 104      ;jump if greater than
110  XOR Y, Y
112  JNZ 100      ;jump if no zero
114  SHL Y, 2
116  EXIT
```

1. How much times **JGT**, and **JNZ** instructions to be true?
2. Find the result of **X**, and **Y** at the end of execution?
3. Value of PC depending on the condition of **JNZ**?

53- Check on this program suppose all register were 6-bit , and then draw the block diagram that implement these arithmetic operations through the ALU, with explaining how to control the program to perform addition in the case of add and subtract also:

```
MOV C,-25
MOV B,14
ADD C, B
MOV B, 3
SUB C, B
```

54- Find the result of question (53) using weighted sum of the values?

55- Specify PC, IR , MAR and MBR for this instruction, due to the function of each one?

```
200 MOV AX,[BX]
```

56- Write a program in assembly language as 1-address format for this operation ?

```
Y=X/(Z+2*M)
```

57- Design the block diagram that can perform these statement of RTL ;

if T0 copy from R0 to R4; if T1 copy from R1 to R4 ; if T2 copy from R2 to R5 ;

if T3 copy from R3 to R5

58- Design a block diagram capable to concatenate two (n- bit) register to another register (suppose any name of the registers),

59- What is the size of the produced register in question 58?

60- What are the difference between the multiplexor and the encoder (ability to explain by example and truth table)?

61- suppose that a computer system have two level of memory unit L1 is the cache memory have access time $0.02\mu s$; and L2 is the main memory of access time $0.2\mu s$, is the percentage of data occurrence in L1 is 15%, find the average access time ? is the cache benefit in this case explain your answer briefly ?

62- Draw the block diagram of ALU status bits condition using 16 bit operands?

63- Draw the block diagram for the Hierarchy of memory types?

64- Suppose a computer system operate in set associative mode consist of cache memory capacity 512 Kbyte, 256K lines, and 64 K is the number of set in the cache memory, if the tag field size is 4 bit; evaluate :

- Number of line in each set (set size)?
- Memory organization address field?
- Size of main memory?
- Number of block in main memory?

65- If there are 16 K line in the cache memory, evaluate the line address of the following main memory address field in a direct addressing mapping, where the word field consist of 2 bit:

- a) FF339C (H)
- b) E2AA31 (H)
- c) 001110 (H)
- d) 123456 (H)

66- Testing on this sub program; then answer the following questions:

- a) How many times the statements between the brackets to be executed?
- b) What is the operation performed by this program.
- c) Which addressing format used to access the memory?

```

MOV R1,20

MOV R2, 10

MOV R3, 0

back:  ADD R3, [R1]
      INC R1
      DEC R2
      JNZ back
  
```

67- write a program using GPR language that performs the following computation, assuming that all registers start out containing '0' the final result may be saved in any register.

$$(11*2)+(7\backslash(22+3))$$

68- The destination 8-bit operand of ALU to be checked for zero's output and saved in the Z flag, Suppose the circuit diagram used to produce it (Z flag), describe your answer?

69- Suppose a computer system operate in set associative mode consist of cache memory capacity 512 Kbyte, and main memory capacity 2 Mbyte, and the main memory splitting to blocks, each block consist of 2 words. Compute the organization of the main memory address field if there are 4 line in each set; (k=4)? And also find the number of blocks in main memory?

70- Draw the circuit diagram that used to implement bidirectional (4-bit) shift register, using specific type of MUX, describe the direction of shift how to be controlled?

71- Using stack algorithm steps convert the following formula from infix to postfix:
 $Y=(A+B+C)*(D\backslash E+F)$

72- Find the result of A/B, if A=10011, B=1011 using algorithm of binary division?

73- Suppose a computer system operate in direct accessing mode consist of tow level of memory (L1) are cache memory capacity 256 Kbyte, (L2) are main memory capacity 4 Mbyte, and the main memory splitting to blocks, each block consist of 8 words.

Compute the following:

- i- The organization of the main memory address field.
- ii- The number of blocks in main memory.
- iii- The number of lines in cache memory.

74- : Design general register organization system that performs 64 micro operations using 4 register (R1, R2, R3 and R4) in the CPU? And clarify the control word for selection the instruction field? (Hint use specific size of MUX)?

75- Suppose an ALU throughout the processor implement operations between tow operands A and B (5bit each), draw the circuit diagram of the subsequent arithmetic micro operations ($F = A+B$, $F = B-A$, $F=A-1$ and $F=B-1$) using the specific logic circuit?

76- let the dividend d A equal (10101) and the divisor B equal (0100), using the algorithm of division evaluate the quotient and the remainder of A/B?

77- Given the following memory values and CPU registers (Accumulator, R1,R2, and R3): Word 20 contains 40, Word 30 contains 50, Word 40 contains 60, Word 50 contains 70, R1 contains 30, R2 contains 50, R3 contains 10, Accumulator contains 0

LOAD IMMEDIATE 20
LOAD DIRECT 20
LOAD INDIRECT 20
LOAD DIRECT R1
LOAD INDDIERECT R2
ADD Acc with R3

i)what values do the following instructions load in to the accumulator?

ii) write these instruction as assembly language formula?

78- For the following sequence of instructions write the Arithmetic expression that implemented by the following assembly program?, By which addressing format these instruction to be executed, clarify each one?

PUSH A
PUSH B
PUSH C
PUSH D
PUSH E
ADD
PUSH F
DIV
ADD
PUSH G
SUB
PUSH H
DIV
MUL
ADD
POP X

79- Suppose a memory address mapping of 2048 Byte Main Memory which have been distributed in to two equal parts of (ROM, and RAM) type, if you have the following chip organization (256 Byte RAM chip, and 512 Byte ROM chip).

Analyze this system and solve the following points:

1. Draw the ROM, and RAM chip?
2. Specify the table of address with rang of memory location for each one?
3. Memory chips architecture connections with the CPU?

80- Design the circuit diagram that implement the following notations (in the case of 8 bit registers)?

T0: R3 ← R1
T1: R3 ← R2
T2: R4 ← R1
T3: R4 ← R2