Chapter Six (2nd Semester)
Bipolar Junction Transistor

6.1: Introduction

John Bardeen, **Walter Brattain**, and **William Shockley** invented the first working transistors at Bell Labs, the point-contact transistor in 1947. Shockley introduced the improved bipolar junction transistor in 1948, which entered production in the early 1950s and led to the first widespread use of transistors.

The three physicists who invented the transistor; **William Shockley**, **John Bardeen**, and **Walter Brattain** were awarded with the **Nobel Prize**.

First transistor (replica), Bell Labs, 1947.

Two basic types of transistors are the **bipolar junction transistor (BJT)**, which we will begin to study in this chapter, and the **field-effect transistor (FET)**, which we will cover in later chapters. The BJT is used in two broad areas-as a **linear amplifier** to boost or amplify an electrical signal and as an **electronic switch**. Both of these applications are introduced in this chapter.

6.2: Transistor Structure

The **BJT** (**Bipolar Junction Transistor**) **is constructed with three doped semiconductor regions separated by two *pn* junctions**, as shown in the epitaxial planar structure in Figure (la).

The **three regions** are called **emitter**, **base**, and **collector**.

Physical representations of the **two types of BJTs** are shown in Figure (lb) and (lc). **One type consists of two *n* regions separated by a *p* region (*npn*)**, and the **other type consists of two *p* regions separated by an *n* region (*pnp*)**.

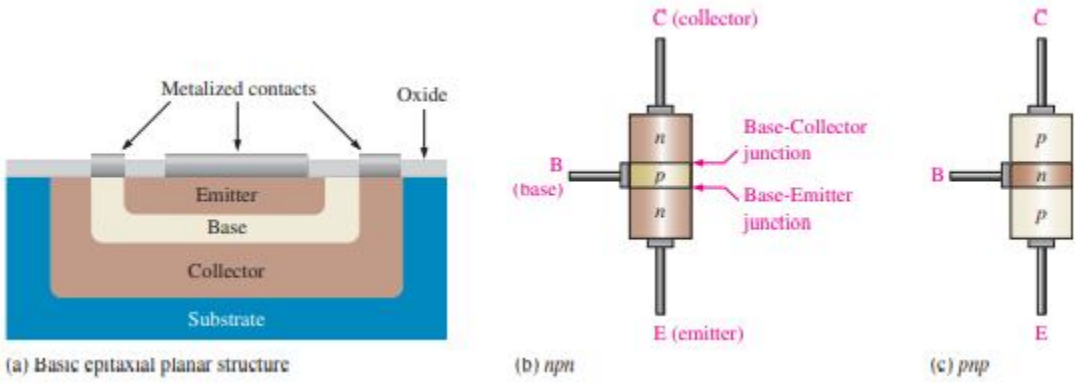


Figure (1): Basic BJT construction.

The *pn* junction joining the base region and the emitter region is called the ***base-emitter junction***.
The *pn* junction joining the base region and the collector region is called the ***base-collector junction***, as indicated in Figure (1b).

A wire lead connects to each of the three regions, as shown. These leads are labeled **E**, **B**. and **C** for **emitter**, **base**, and **collector** respectively.

The **base** region **is lightly doped** and **very thin** compared to the **heavily doped emitter** and the **moderately doped collector** regions. (The reason for this is discussed in the next section.)

Figure (2) shows the schematic symbols for the ***npn*** and ***pnp*** bipolar junction transistors. The term bipolar refers to the use of both **holes** and **electrons** as carriers in the transistor structure.

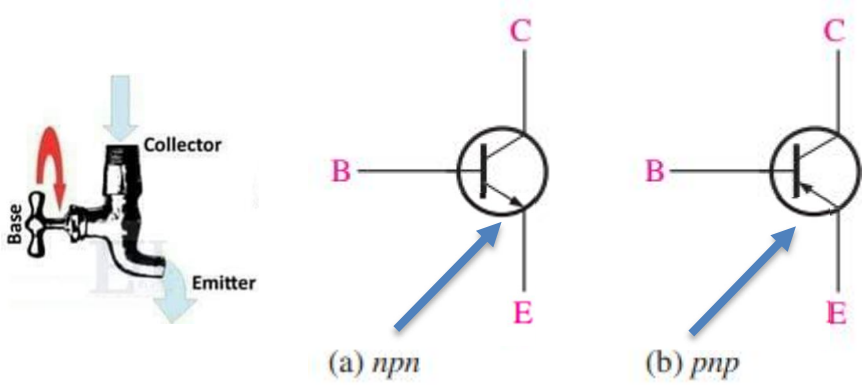


Figure (2): Standard BJT (bipolar junction transistor) symbols.

6.3: Basic Transistor Operation

6.3.1: Biasing

Figure (3) shows the proper bias arrangement for both ***npn*** and ***pnp*** transistors for active operation as an **amplifier**.

Notice that in both cases the **base-emitter (BE) junction** is ***forward-biased*** and the **base-collector (BC) junction** is ***reverse-biased***.

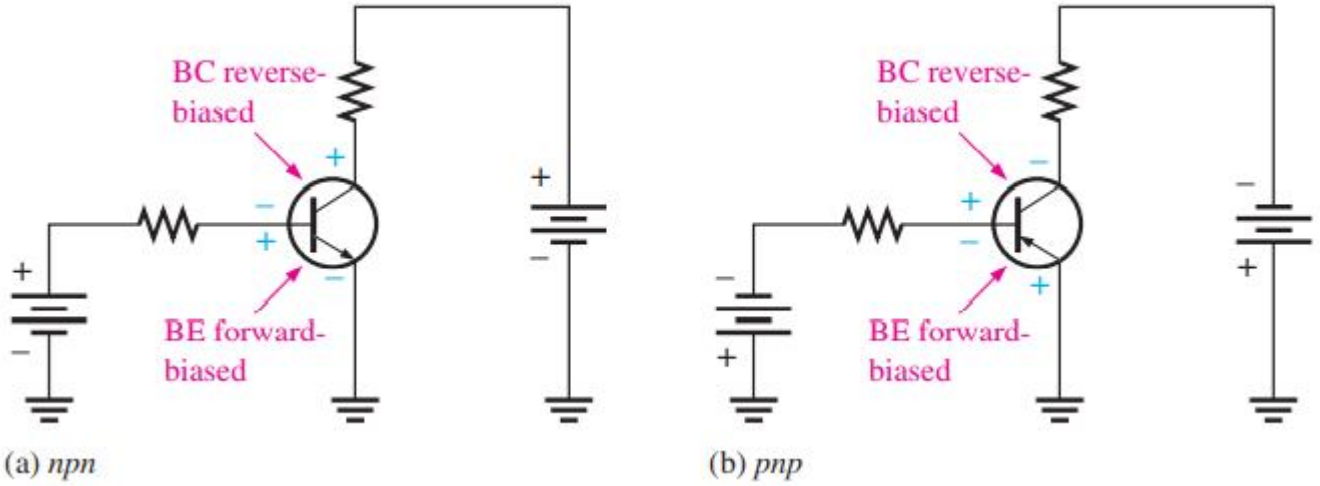


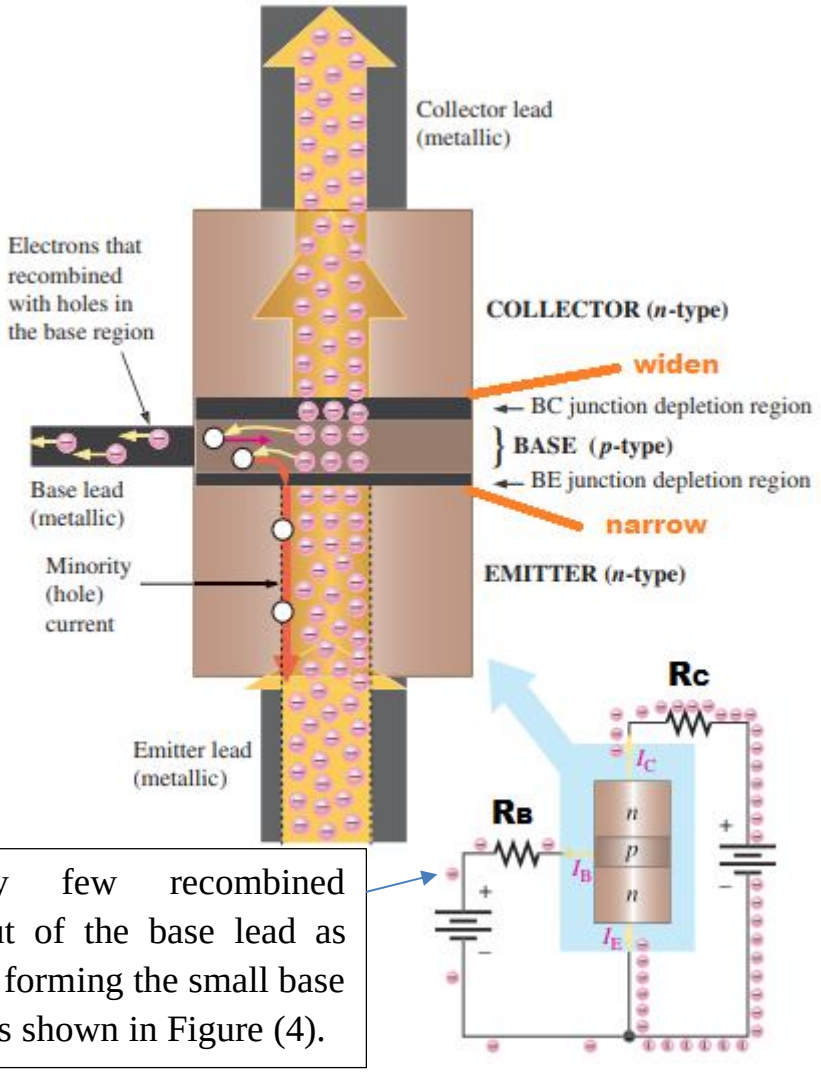
Figure (3): Forward-reverse-bias of a BJT.

6.3.2: Operation

To illustrate transistor action let's examine what happens inside the ***npn*** transistor. The ***forward-bias*** from base to emitter **narrows** the BE depletion region, and the ***reverse-bias*** from base to collector **widens** the BC depletion region, as depicted in Figure (4).

The **heavily doped** $n-type$ **emitter** region is teeming **with** conduction band (free) **electrons** that **easily diffuse** through the forward-biased BE junction **into the** $p-type$ **base** region where they **become minority carriers**, just as in a *forward-biased* diode.

The **base region is lightly doped and very thin** so that **it has a limited number of holes**. Thus, only a **small percentage** of **all the electrons** flowing through the BE junction **can combine with** the available **holes in the base**.



These relatively few recombined electrons flow out of the base lead as valence electrons, forming the small base electron current, as shown in Figure (4).

Figure (4): Illustration of BJT action.

Most of the electrons flowing from the emitter into the thin lightly doped base region **do not recombine hut diffuse** into the BC depletion region.

Once in this region, they are **pulled** through the *reverse-biased* BC junction by the **electric field set up** by the force of attraction **between the positive and negative ions**.
Actually, you can think of the **electrons** as being **pulled** across the *reverse-biased* BC junction by the attraction of the **collector supply voltage**.

The **electrons now move** through the collector region, out through the collector lead, and **into the positive terminal** of the collector voltage source. This forms the collector electron current, as shown in Figure (4).

The **collector current** is **much larger than** the **base current**. This is the reason transistors exhibit current gain.

6.3.3: Transistor Currents

The directions of the currents in an *npn* transistor and its schematic symbol are as shown in Figure (5a); those for a *pnp* transistor is shown in Figure (5b).
Notice that the arrow on the emitter of the transistor symbols points in the direction of conventional current.

These diagrams show that the **emitter current (I_E)** is the **sum** of the **collector current (I_C)** and the **base current (I_B)**, expressed as follows:

$$I_E = I_C + I_B \quad \text{... (1)}$$

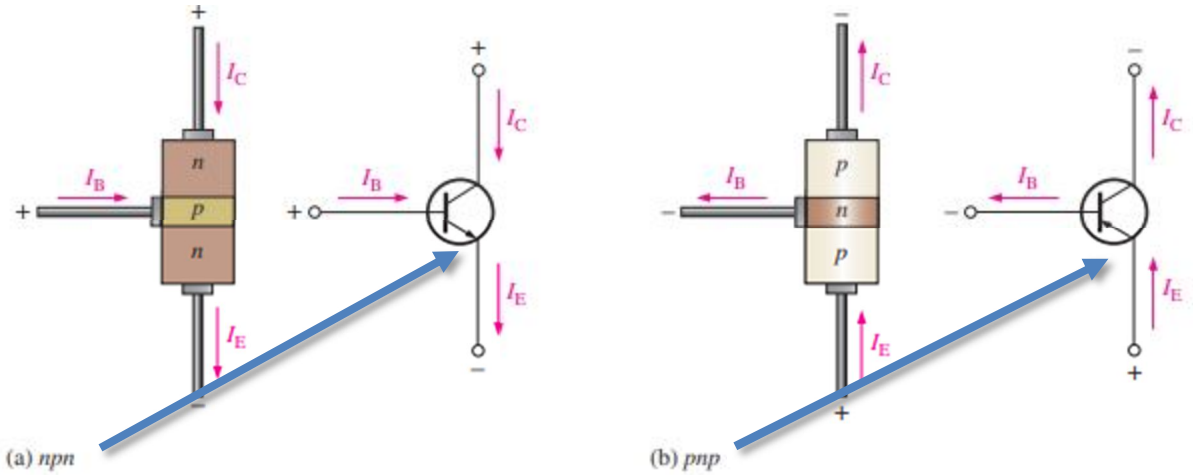


Figure (5): Transistor currents.

6.4: Transistor Characteristics and Parameters

As discussed in the last section, when a **transistor** is **connected** to ***dc*** **bias voltages**, as shown in Figure (6) for both *npn* and *pnp* types.
***V_{BB} forward-biases* the base-emitter junction**, and
***V_{CC} reverse-biases* the base-collector junction**.

Although in this chapter we are using **battery symbols to represent the bias voltages**, in practice the **voltages** are often derived from a ***dc*** **power supply**.

For example; $\boldsymbol{V_{CC}}$ is normally **taken directly from the power supply output** and
$\boldsymbol{V_{BB}}$ (which is smaller) can be **produced with a voltage divider**.
Bias circuits are examined thoroughly in Chapter 7.

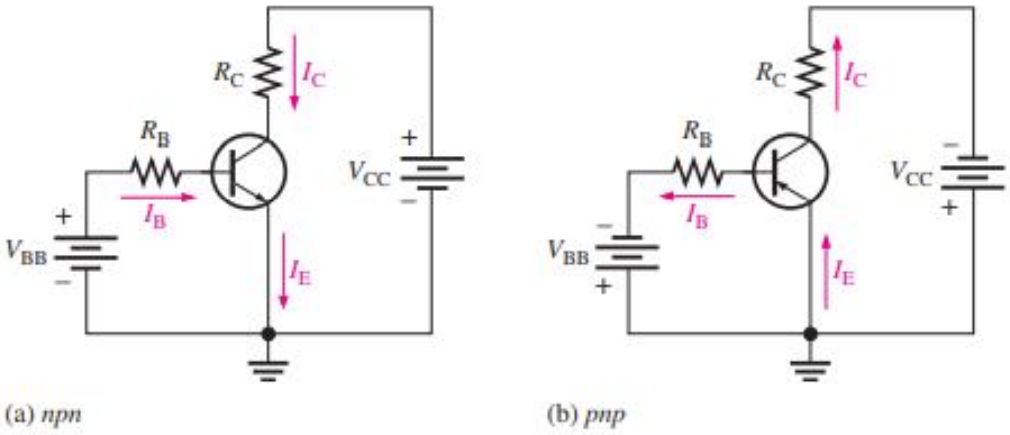


Figure (6): Transistor dc bias circuits

DC Beta (β_{DC}) and DC Alpha (α_{DC}):

The **ratio of the *dc* collector current (I_C) to the dc base current (I_B)** is the ***dc* beta (β_{DC})**, which is the ***dc* current gain** of a transistor.

$$\beta_{DC} = \frac{I_C}{I_B} \quad \text{... (2)}$$

Typical values of β_{DC} range from less than 20 to 200 or higher.
β_{DC} is usually designated as an equivalent hybrid (h) parameter (h_{FE}), on transistor data sheets. All you need to know now is that:

$$h_{FE} = \beta_{DC}$$

The **ratio of the *dc* collector current (I_C) to the *dc* emitter current (I_E)** is the ***dc* alpha (α_{DC})**. The alpha is a **less-used parameter than** beta in transistor circuits.

$$\alpha_{DC} = \frac{I_C}{I_E} \quad \text{... (3)}$$

Typically, values of α_{DC} range from 0.95 to 0.99 or greater, but α_{DC} is always less than 1. The **reason** is that I_C is always slightly less than I_E by the amount of I_B.

For example, if I_E =100 mA and I_B = 1mA, then I_C = 99 mA and α_{DC} = 0.99.

Example 1: Determine β_{DC} and I_E for a transistor where I_B = 50 µA and I_C = 3.65 mA.

Solution:

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.65 \times 10^{-3}}{50 \times 10^{-6}} = 73$$

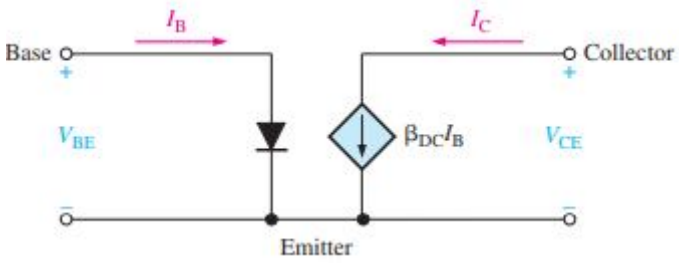
$$I_E = I_C + I_B = 3.65 + \frac{50}{1000} = 3.7\ mA$$

H.W: Q1: A certain transistor has a β_{DC} of 200. When the base current is 50 µA, determine the collector current.

Solution:

Solution:

6.5: Current and Voltage Analysis



Ideal *dc* model of an *npn* transistor.

Consider the basic transistor bias circuit configuration in Figure (7). Three transistors *dc* currents and three *dc* voltages can be identified.

I_B: *dc* base current
I_E: *dc* emitter current
I_C: *dc* collector current
V_{BE}: *dc* voltage at base with respect to emitter
V_{CB}: *dc* voltage at collector with respect to base
V_{CE}: *dc* voltage at collector with respect to emitter
V_{BB}: forward-biases the *base-emitter* junction, and
V_{CC}: reverse-biases the *base-collector* junction.

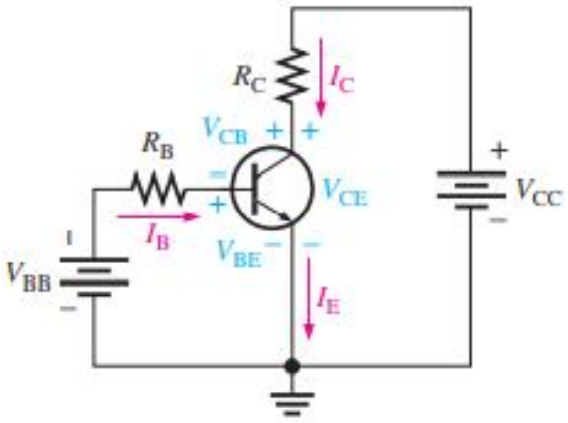


Figure (7): Transistor currents and voltages.

When the base-emitter junction is forward-biased, it is like a **forward-biased diode** and has a nominal **forward voltage drop of V_{BE} = 0.7 V**.

Although in an **actual transistor V_{BE} can be as high as 0.9 V** and is dependent on current. We will use 0.7 V throughout this text in order to simplify the analysis of the basic concepts.

Since the emitter is at ground (0V), by Kirchhoff's voltage law, **the voltage across R_B is**:

$$V_{R_B} = V_{BB} - V_{BE}$$

Also, by Ohm's law; $V_{R_B} = I_B R_B$

Substituting for V_{RB} yields: $V_{R_B} = V_{R_B}$

$$I_B R_B = V_{BB} - V_{BE}$$

Solving for I_B;

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \quad \dots (4)$$

The **voltage at the collector with respect to the grounded emitter is**:

$$V_{CE} = V_{CC} - V_{R_C}$$

Since the drop across R_C is: $V_{R_C} = I_C R_C$

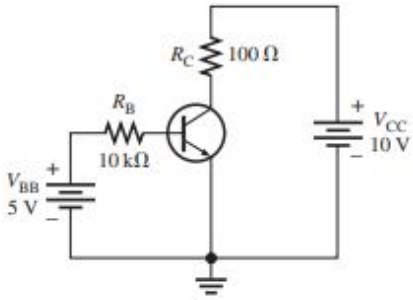
The voltage at the collector can be written as: $V_{CE} = V_{CC} - I_C R_C \dots (5) \rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$

where $I_C = \beta_{DC} I_B$.

The **voltage across the reverse-biased collector-base junction is**:

$$V_{CB} = V_{CE} - V_{BE} \quad \dots (6)$$

Example 2: Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit of this figure. The transistor has a $\beta_{DC} = 150$.



Solution:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 - 0.7}{10 \times 10^3} = 0.43\ mA$$

$$\beta_{DC} = \frac{I_C}{I_B} \rightarrow I_C = \beta_{DC} I_B = 150 \times 0.43 = 64.5\ mA$$

$$I_E = I_C + I_B = 64.5 + 0.43 = 64.93\ mA$$

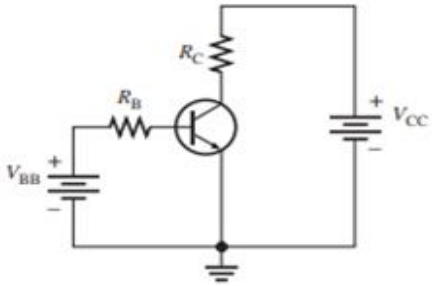
$$V_{BE} = 0.7\ V$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - (64.5 \times 10^{-3} \times 100) = 10 - 6.45 = 3.55\ V$$

$$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = 2.85\ V$$

Since the collector is at a higher voltage than the base, the collector-base junction is reverse-biased.

H.W: Q3: Determine I_B, I_C, I_E, V_{CE}, and V_{CB} in this figure for the following values:
$R_B = 22\,K\Omega$, $R_C = 220\,\Omega$, $V_{BB} = 6\,V$, $V_{CC} = 9\,V$, and $\beta_{DC} = 90$.



Solution:

6.6: Transistor Configuration and Characteristics

A **bipolar transistor can be connected in three different arrangements** which are expressed by the following **three transistor configurations**:

1. **Common base configuration**
2. **Common emitter configuration**
3. **Common collector configuration**

In the common base configuration, the **base** is **common (grounded)** to the **input** and **output**. The **input** is applied **between the emitter and base** and the **output** is taken across the **collector and base**.

In **common emitter** and **common collector** configurations, the **emitter** and the **collector** are respectively **grounded**.

The **three transistor configurations** are shown in figure (8). The input and output impedances and characteristics of a transistor are different for the three configurations.

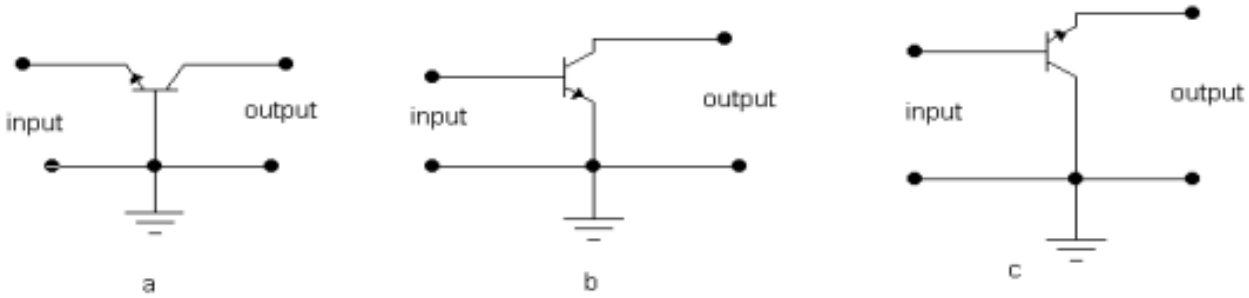


Figure (8): An *pnp* transistor in (a) common base (b) common emitter (c) common collector.

In any transistor configuration, **one deals** with **four** different parameters, **input current**, **input voltage**, **output current**, and **output voltage**.
A number of families of characteristic curves can be obtained from these parameters.

Generally, **two types of characteristics** are of importance input characteristics and output characteristics. A family of curves expressing the **relationship between input current and input voltage for different output voltages** is called **input characteristics**. Similarly, the **output characteristics** refer to a family of curves expressing the **relationship between output voltage and output current for different input currents**.

A transistor may exhibit **different characteristic curves** when operated under the **effect of *dc* voltages only** and under the **combined effect of *ac* input signal and *dc* electrode potentials** as in actual operating conditions.

The characteristics obtained in the former case are called the **static characteristics** and those obtained in the latter case are called the **dynamic characteristics**.

In this section we shall consider the static characteristics of common base, common emitter and common collector configurations.

6.6.1: Common Base Static Characteristics

The characteristic diagram of determining the common base characteristic is shown in the figure (9).

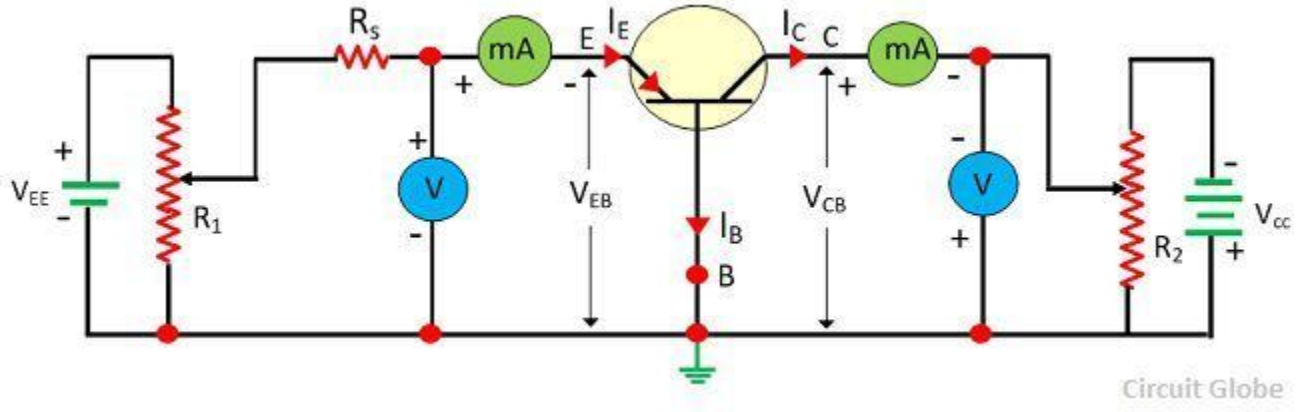


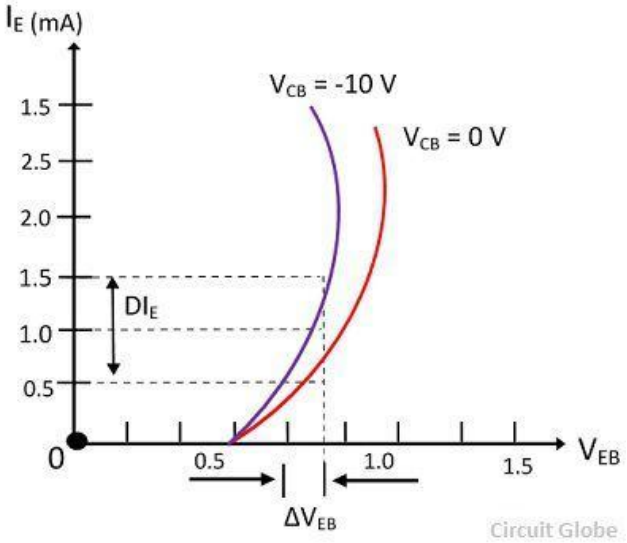
Figure (9): Circuit diagram to static characteristics for a CB *pnp* transistor.

The emitter to base voltage V_{EB} can be varied by adjusting the potentiometer R_1.
A series resistor $\boldsymbol{R_s}$ is inserted in the emitter circuit **to limit the emitter current $\boldsymbol{I_E}$.**
The **value of the emitter** changes to a large value even if the value of a potentiometer slightly changes.
The **value of collector voltage** changes slightly by changing the value of the potentiometer R_2.
The input and output characteristic curve of the potentiometer explains below in details.

Input or Emitter Characteristics Curve:

The curve plotted between emitter current $\boldsymbol{I_E}$ and the emitter-base voltage $\boldsymbol{V_{EB}}$ at **constant collector-base voltage $\boldsymbol{V_{CB}}$** is called input characteristic curve.

The input characteristic curve is shown in the figure right.



The following points are taken into consideration from the characteristic curve:

1. For a specific value of V_{CB}, the *curve* is a diode characteristic in the forward region. The PN emitter junction is *forward-biased*.
2. *When* the value of the voltage base current increases the value of emitter current increases slightly. The junction behaves like a *better diode*. The emitter and collector current are *independent* of the collector-base voltage V_{CB}.
3. The emitter current I_E increases with the small increase in emitter-base voltage V_{EB}. It shows that *input resistance is small*.

Input Resistance:

The ratio of change in emitter-base voltage to the resulting change in emitter current **at constant** collector-base voltage V_{CB} is known as input resistance.
The input resistance is expressed by the formula:

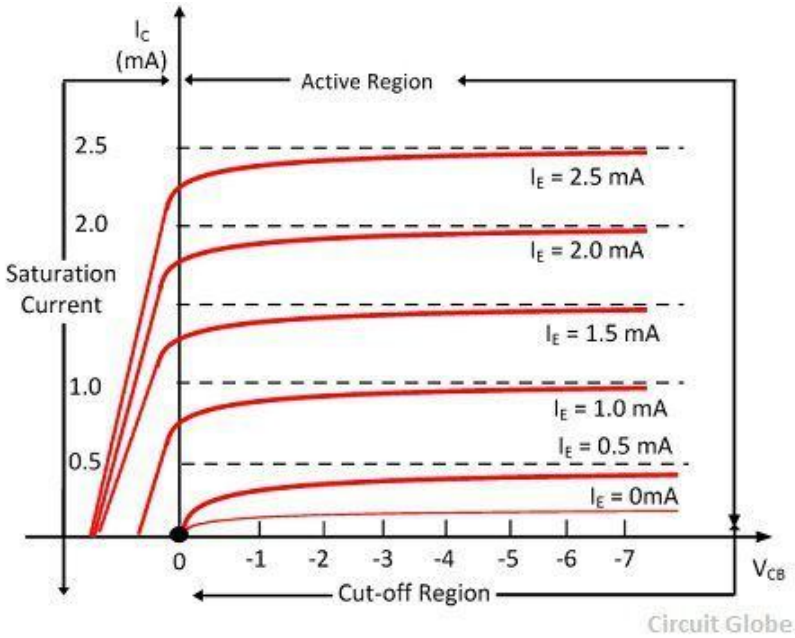
$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad at \text{ constant } V_{CB}$$

The value of emitter-base voltage V_{EB} **increases** *with* the **increases** in the emitter-base current I_E. The **value of input resistance is very low**, and their value may vary **from a few ohms to 10 Ω**.

Output Characteristic Curve:

In common base configuration, the curve plotted between the collector current $\boldsymbol{I_C}$ and collector-base voltage $\boldsymbol{V_{CB}}$ at **constant** emitter current $\boldsymbol{I_E}$ is called output characteristic.

The CB configuration of PNP transistor is shown in the figure right.



The following points from the characteristic curve are taken into consideration:

1. The *active region* of the collector-base junction is *reverse-biased*, the collector current $\boldsymbol{I_C}$ **is almost equal to the emitter current** $\boldsymbol{I_E}$. The transistor is always operated in this region.
2. The *curve* of the active regions is **almost flat**. The large charges in V_{CB} produce only a tiny change in I_C The circuit has very **high output resistance** $\boldsymbol{r_o}$.
3. *When* V_{CB} is positive, the collector-base junction is **forward-bias** and the collector current decrease suddenly. This is the saturation state in which the collector current does not depend on the emitter current.
4. *When* **the emitter current is zero, the collector current is not zero**. The current which flows through the circuit **is the reverse leakage current, i.e.,** $\boldsymbol{I_{CBO}}$. **The current is temperature depends** and its value range **from** $\boldsymbol{0.1\ to\ 1.0\ \mu A}$ **for silicon transistor** and $\boldsymbol{2\ to\ 5\ \mu A}$ **for germanium transistor**.

Output Resistance:

The ratio of change in collector-base voltage to the change in collector current **at constant** emitter current $\boldsymbol{I_E}$ is known as output resistance $\boldsymbol{r_o}$.

$$\boldsymbol{r_o} = \frac{\Delta V_{CB}}{\Delta I_C} \ \boldsymbol{at}\ \textbf{constant}\ \boldsymbol{I_E}$$

The output characteristic of the change in collector current I_C is **very little** *with* the change in collector-base voltage V_{CB}. The **output resistance is very high** of the order of several kilo-ohms.

Current Amplification factor (α):

$$\boldsymbol{\alpha} = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_E - \Delta I_B}{\Delta I_E} = 1 - \frac{\Delta I_B}{\Delta I_E}$$

Total Collector Current (I_C):

$$\boldsymbol{I_C} = \alpha I_E + I_{leakage}$$
$$\boldsymbol{I_C} = \alpha I_E + I_{CBO}$$

6.6.2: Common Emitter Static Characteristics

The characteristic of the common emitter transistor circuit is shown in the figure (10).

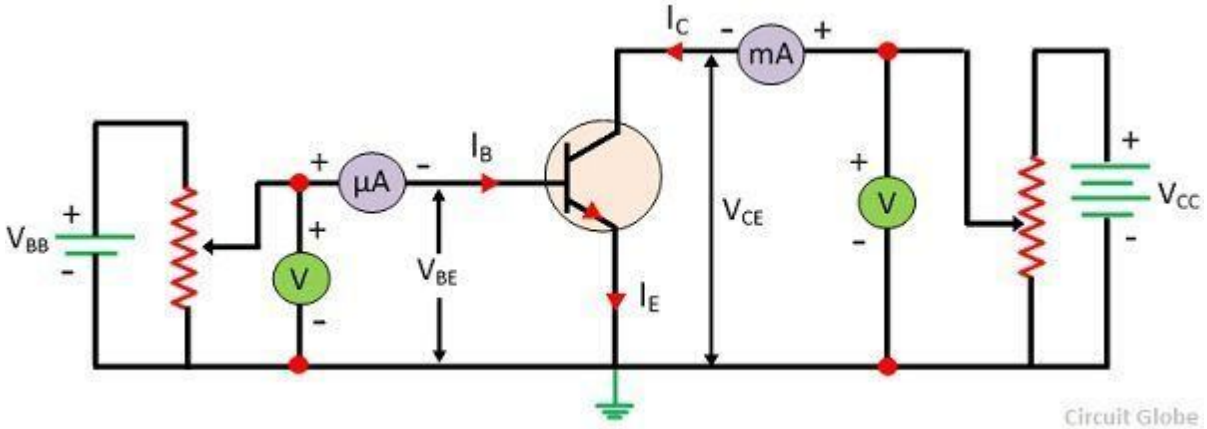


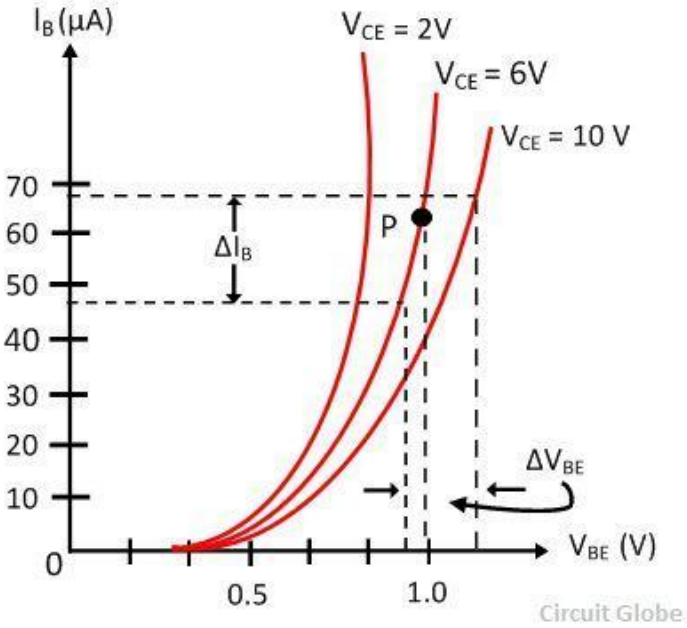
Figure (10): Circuit diagram to static characteristics for a CE *npn* transistor.

The base to emitter voltage V_{BE} varies by adjusting the potentiometer R_1.
And the collector to emitter voltage V_{CE} varied by adjusting the potentiometer R_2.
For the various setting, the current and voltage are taken from the milliammeters and voltmeters. On the basis of these readings, the input and output curves are plotted on the curve.

Input Characteristics Curve:

The curve plotted between base current $\boldsymbol{I_B}$ and the base-emitter voltage $\boldsymbol{V_{BE}}$ is called Input characteristics curve.

For drawing the input characteristic, the reading of base currents is taken through the ammeter on emitter voltage V_{BE} at constant collector-emitter voltage (V_{CE}). The curve for different value of collector-emitter voltage is shown in the figure right.



The curve for common base configuration is similar to a *forward diode characteristic*.
The base current $\boldsymbol{I_B}$ **increases** *with* the **increases** in the emitter-base voltage V_{BE}.
Thus, the **input resistance** of the CE configuration is comparatively **higher** that of CB configuration.
The effect of CE *does not* cause large deviation on the curves, and hence the effect of a change in V_{CE} on the input characteristic is ignored.

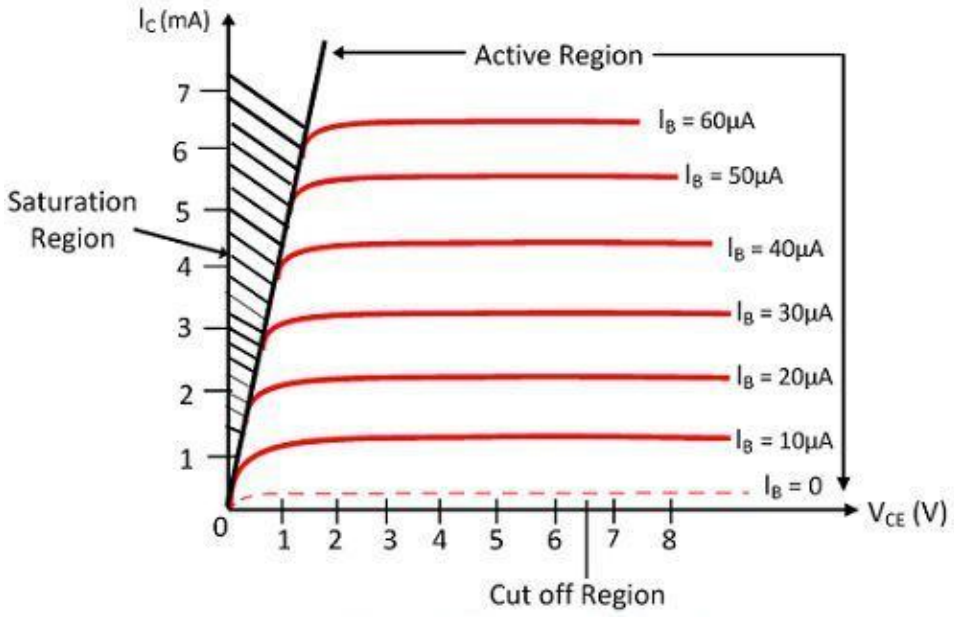
Input Resistance:

The ratio of change in base-emitter voltage V_{BE} to the change in base current ΔI_B at constant collector-emitter voltage V_{CE} is known as input resistance, i.e.,

$$\boldsymbol{r_i = \frac{\Delta V_{BE}}{\Delta I_B} \ \ at \ constant \ V_{CE}}$$

Output Characteristics Curve:

In CE configuration the curve draws between collector current $\boldsymbol{I_C}$ and collector-emitter voltage $\boldsymbol{V_{CE}}$ at a **constant** base current $\boldsymbol{I_B}$ is called output characteristic.
The characteristic curve for the typical NPN transistor in CE configuration is shown in the figure below.



In the *active region*, the collector current I_C **increases slightly** as collector-emitter V_{CE} current increases. The **slope** of the curve **is quite more than** the output characteristic of CB configuration. The **output resistance** of the common base connection **is more than** that of CE connection.

The value of the collector current $\boldsymbol{I_C}$ *increases with* the *increase* in $\boldsymbol{V_{CE}}$ **at constant** voltage $\boldsymbol{I_B}$, the value $\boldsymbol{\beta}$ of also *increases*.

When the V_{CE} **falls**, the I_C also **decreases** rapidly. The collector-base junction of the transistor always in forward bias and work saturate. In the saturation region, the collector current becomes independent and free from the input current I_B.

In the *active region* $\boldsymbol{I_C = \beta I_B}$, a **small** current $\boldsymbol{I_C}$ is not zero, and it **is equal to reverse leakage current** $\boldsymbol{I_{CEO}}$.

Output Resistance:

The ratio of change in collector- emitter voltage to the change in collector current **at constant** base current $\boldsymbol{I_B}$ is known as output resistance r_o.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \; at \; \textbf{constant } I_B$$

The **value of output resistance** of CE configuration **is more than** that of CB.

Base Current Amplification Factor (β):

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_E - \Delta I_B}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_B} - 1$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \div \frac{\Delta I_E}{\Delta I_E} = \frac{\frac{\Delta I_C}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1 - \alpha}$$

Total Collector Current (I_C):

$$I_C = \beta I_B + I_{CEO}$$

6.6.3: Common Collector Static Characteristics

In common collector configuration circuit is shown in figure (11). Here collector is grounded and it is used as the common terminal for both input and output. It is also called as grounded collector configuration. Base is used as an input terminal whereas emitter is the output terminal.

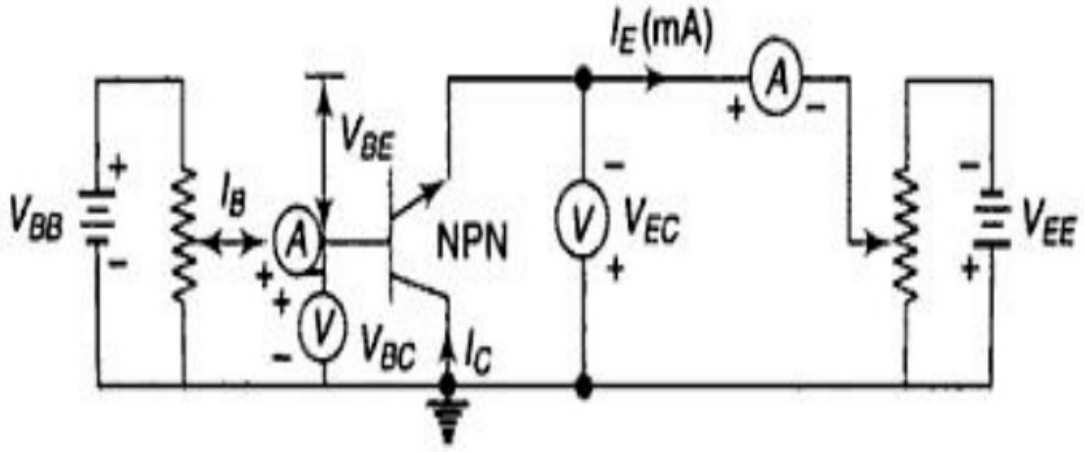
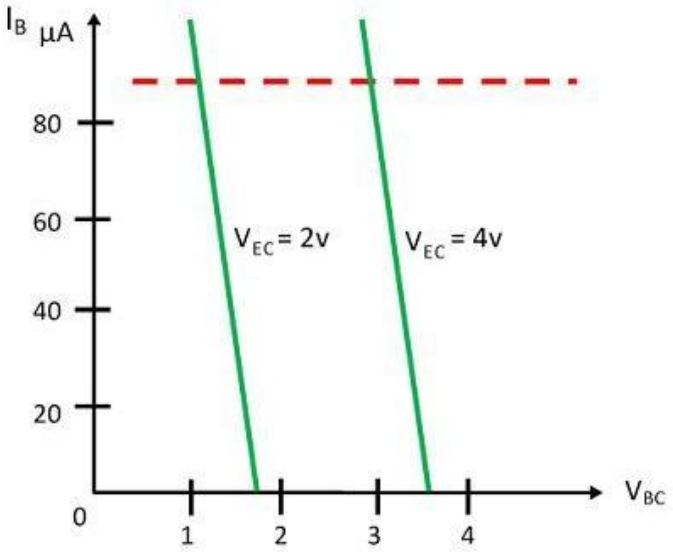


Figure (11): Circuit diagram to static characteristics for a CC *npn* transistor.

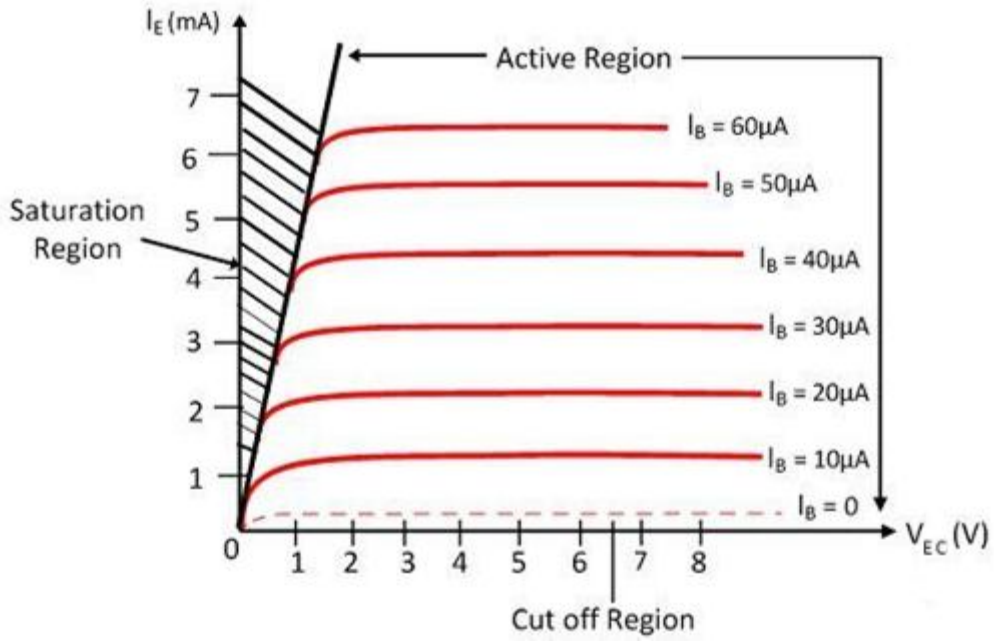
Input Characteristics Curve:

The input characteristic of the common collector configuration is drawn between collector-base voltage $\boldsymbol{V_{BC}}$ and base current $\boldsymbol{I_B}$ at **constant** emitter current voltage $\boldsymbol{V_{EC}}$. The value of the output voltage V_{EC} changes with respect to the input voltage V_{BC} and I_B with the help of these values, input characteristic curve is drawn. The input characteristic curve is shown below.



Output Characteristics Curve:

The output characteristic of the common emitter circuit is drawn between the emitter-collector voltage $\boldsymbol{V_{EC}}$ and output current $\boldsymbol{I_E}$ at **constant** input current $\boldsymbol{I_B}$. If the input current $\boldsymbol{I_B}$ is zero, then the collector current $\boldsymbol{I_E}$ also becomes zero, and no current flows through the transistor.



The transistor operates in active region when the base current increases and reaches to saturation region. The graph is plotted by keeping the base current I_B constant and varying the emitter-collector voltage V_{EC}, the values of output current I_E is noticed with respect to V_{EC}. By using the V_{EC} and I_E at constant I_B the output characteristic curve is drawn.

Current Amplifier Factor (γ):

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} \div \frac{\Delta I_E}{\Delta I_E} = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$$

6.7: Collector Characteristic Curves

Using a ***circuit*** like that shown in Figure (12a), you can ***generate*** a set of **collector characteristic curves** that show how the collector current, I_C varies with the collector-to-emitter voltage (V_{CE}) for specified values of base current (I_B) Notice in the circuit diagram that both V_{BB} **and** V_{CC} **are** ***variable*** **sources of voltage**.

Assume that V_{BB} is set to produce a certain value of I_B and V_{CC} is zero. For this condition, both the **base-emitter junction** and the **base-collector junction** are ***forward-biased*** because the ***base*** is at approximately ***0.7 V*** while the **emitter** and the **collector** are at ***0 V***.

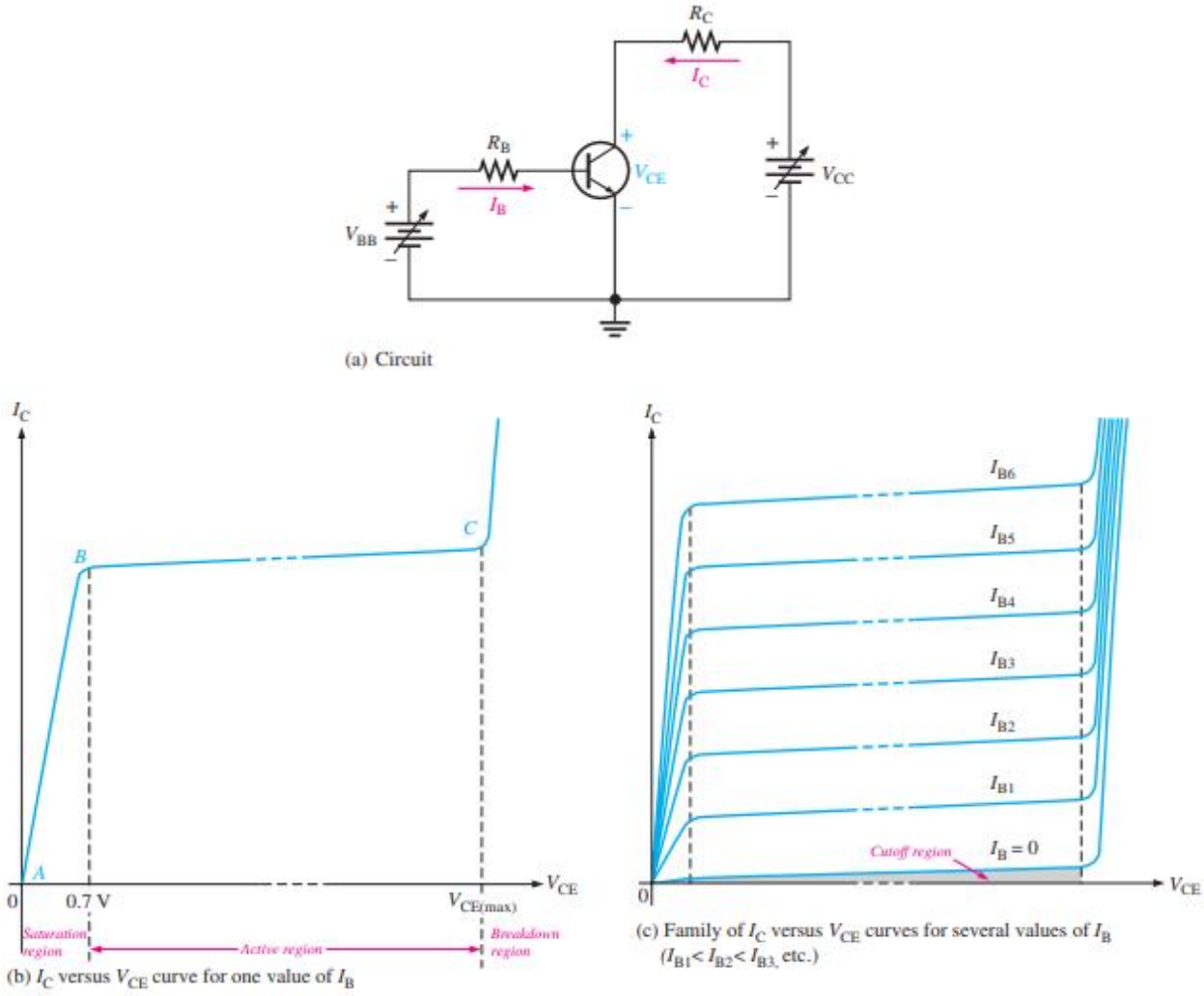


Figure (12): Collector characteristic curves.

The base current is through the base-emitter junction because of the low impedance path to the ground and therefore, I_C **is zero**. When both junctions are forward-biased, the **transistor is in the saturation region** of its operation.

As V_{CC} **is increased**, V_{CE} **increases gradually** as the collector current (I_C) **increases**. This is indicated by the portion of the characteristic curve between points A and B in figure (12b).

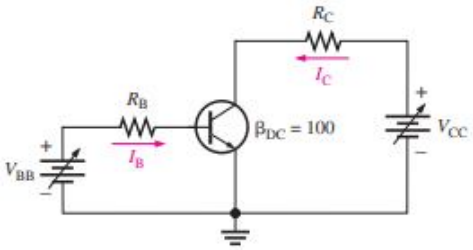
I_C **increases** as V_{CC} **is increased** because V_{CE} **remains less than 0.7 V** due to the *forward-biased base-collector junction*.

Ideally, **when** V_{CE} **exceeds 0.7 V**, the *base-collector junction becomes reverse-biased* and the **transistor goes into the active or linear region** of its operation.
Once the *base-collector junction is reverse-biased*, I_C **levels off** and **remains essentially constant** for a given value of I_B as V_{CE} **continues to increase**.
Actually, I_C **increases very slightly** as V_{CE} **increases** due to the **widening of the base-collector depletion region**.
This results in **fewer holes** for **recombination** in the **base region** which effectively causes a **slight increase in** β_{DC}. This is shown by the portion of the characteristic curve between points B and C in Figure (12b).
For this portion of the characteristic curve, the value of I_C **is determined only** by the relationship expressed as $I_C = \beta_{DC} I_B$.

When V_{CE} **reaches a sufficiently high voltage**, the **reverse-biased base-collector junction goes into breakdown**; and the collector current I_C **increases rapidly** as indicated by the part of the curve to the right of point C in Figure (12b). **A transistor should never be operated (used) in this breakdown region**.

A **family of collector characteristic curves** is produced when I_C versus V_{CE} is plotted for **several values of** I_B, as illustrated in Figure (12c).
When $I_B = 0$, the **transistor is in the cutoff region** although there is a **very small collector leakage current** as indicated.
The amount of collector leakage current for $I_B = 0$ is ***exaggerated*** on the graph for illustration.

Example 3: Sketch an ideal family of collector curves for the circuit in this figure for I_B= 5μA to 25 μA in 5 μA increments. Assume β_{DC}= 100 and that V_{CE} does not exceed breakdown.

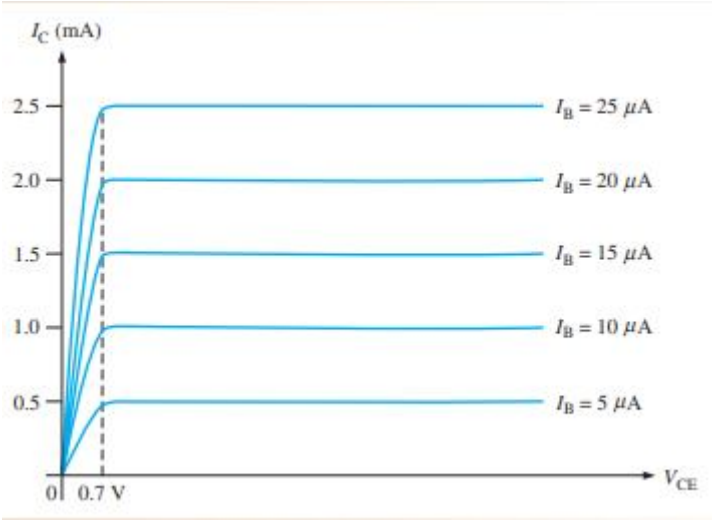


Solution:

Using the relationship $I_C = \beta_{DC} I_B$ values of I_C are calculated.

I_B	I_C
5 μA	0.5 mA
10 μA	1.0 mA
15 μA	1.5 mA
20 μA	2.0 mA
25 μA	2.5 mA

The resulting curves are plotted in this figure. These are ideal curves because the slight increase in I_C for a given value of I_B as V_{CE} increases in the active region is neglected.



6.8: Cut off

As previously mentioned, **when I_B = 0**, the **transistor is in the cutoff region of its operation**. This is shown in Figure (13) with the base lead open. Resulting in a base current **I_B of zero**. Under this condition, there is **a very small amount of collector leakage current I_{CEO}** due mainly to **thermally produced carriers**.

Because **I_{CEO} is extremely small** it will **usually be neglected** in circuit analysis so that **$V_{CE} = V_{CC}$**.

In cutoff, both the **base-emitter** and the **base-collector junctions *are reverse-biased***.

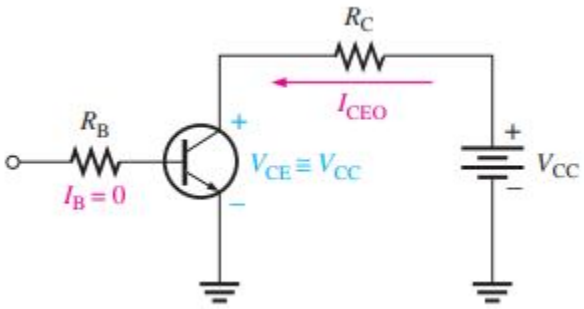


Figure (13): Cutoff: Collector leakage current (I_{CEO}) is extremely small and is usually neglected. Base-emitter and base- collector junctions are reverse biased.

6.9: Saturation

When the **base-emitter junction** becomes **forward-biased** and the base current $\boldsymbol{I_B}$ **is increased**, the collector current $\boldsymbol{I_C}$ **also increases** ($I_C = (\beta_{DC} I_B)$ and $\boldsymbol{V_{CE}}$ **decreases** as a result of more drop across the collector resistor ($\boldsymbol{V_{CE} = V_{CC} - I_C R_C}$). This is illustrated in Figure (14).

When $\boldsymbol{V_{CE}}$ **reaches its saturation value** $\boldsymbol{V_{CE(Sat)}}$, the **base-collector junction** becomes **forward biased** and $\boldsymbol{I_C}$ **can increase no further** even with a **continued increase in** $\boldsymbol{I_B}$.

At the point of saturation, the **relation** $\boldsymbol{I_C = (\beta_{DC} I_B}$ **is no longer valid** $\boldsymbol{V_{CE(Sat)})}$ *for a transistor occurs somewhere below the knee of the collector curves*, and it is usually only a few tenths of a volt for silicon transistors.

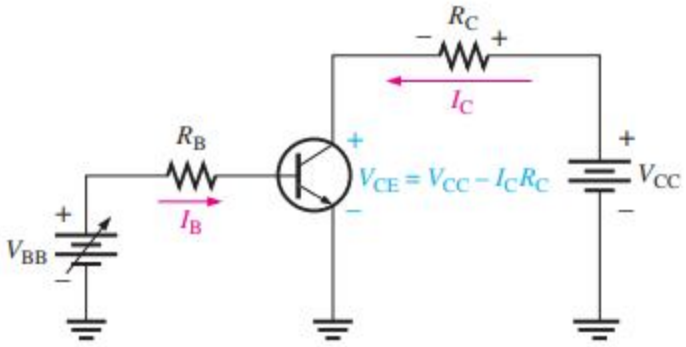


Figure (14): Saturation as I_B increases due to increasing V_{BB}, I_C also increases and V_{CE} decreases due to the increased voltage drop across R_C. When the transistor reaches saturation, I_C can increase no further regardless of further increase in I_B Base-emitter and base-collector junctions are forward-biased.

6.10: DC Load Line

Cutoff and **saturation** can be illustrated in relation to the collector characteristic curves by the **use of a load line**. Figure (15) shows a dc load line drawn on a family of curves connecting the **cutoff point** and the **saturation point**.

The bottom of the load line is at **ideal cutoff** where $\boldsymbol{I_C = 0}$ and $\boldsymbol{V_{CE} = V_{CC}}$.

The top of the load line is at **saturation** where $\boldsymbol{I_C = I_{C(Sat)}}$ and $\boldsymbol{V_{CE} = V_{CE(Sat)}}$.

In between cutoff and saturation along the load line is the active region of the transistor's operation.

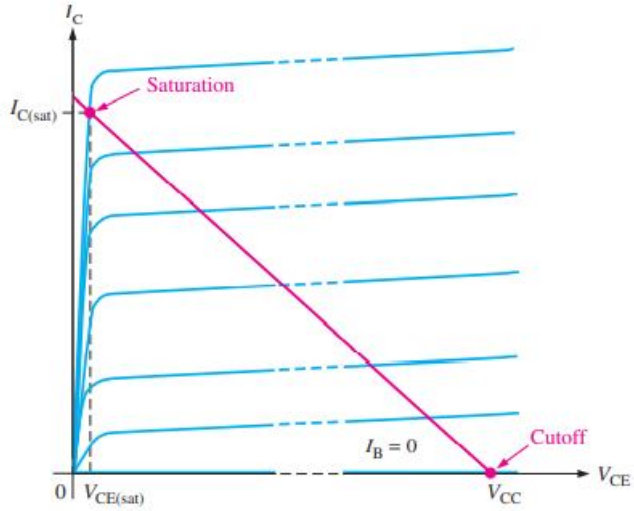
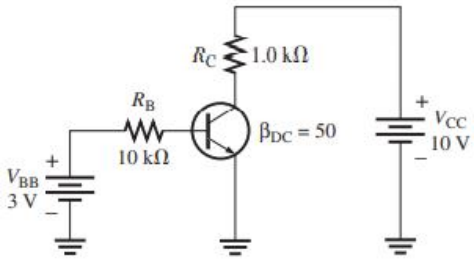


Figure (15): DC load line on a family of collector characteristic curves illustrating the cutoff and saturation conditions.

Example 4: Determine whether or not the transistor in this figure is in saturation. Assume $V_{CE(Sat)} = 0.2\,V$.



Solution:

First, determine $I_{C(Sat)}$:

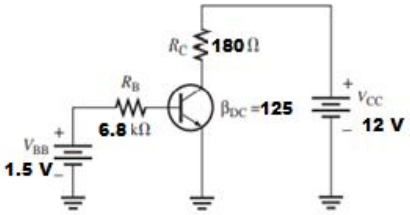
$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10\,\text{V} - 0.2\,\text{V}}{1.0\,\text{k}\Omega} = \frac{9.8\,\text{V}}{1.0\,\text{k}\Omega} = 9.8\,\text{mA}$$

Now, see if I_B is large enough to produce $I_{C(Sat)}$:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3\,\text{V} - 0.7\,\text{V}}{10\,\text{k}\Omega} = \frac{2.3\,\text{V}}{10\,\text{k}\Omega} = 0.23\,\text{mA}$$

$$I_C = \beta_{DC} I_B = (50)(0.23\,\text{mA}) = 11.5\,\text{mA}$$

H.W: Q4: Determine whether or not the transistor in this figure is saturated for the following values: $\beta_{DC} = 125$, $V_{BB} = 1.5\,V$, $R_B = 6.8\,K\Omega$, $R_C = 180\,\Omega$, and $V_{CC} = 12\,V$.



Solution:

6.11: Maximum Transistor Ratings

A **transistor**, like any other electronic device, *has* **limitations** on its operation.
These **limitations** are **stated in the form of maximum ratings** *and* are **normally specified** on the manufacturer's data sheet.
Typically, **maximum ratings** are given for **collector-to-base voltage** V_{CB}, collector-to-emitter voltage V_{CE}, emitter-to-base voltage V_{EB}, collector current I_C, and power dissipation P_D.

The product of V_{CE} and I_C ***must not exceed*** the maximum power dissipation.
Both V_{CE} and I_C ***cannot be maximum*** at the same time.

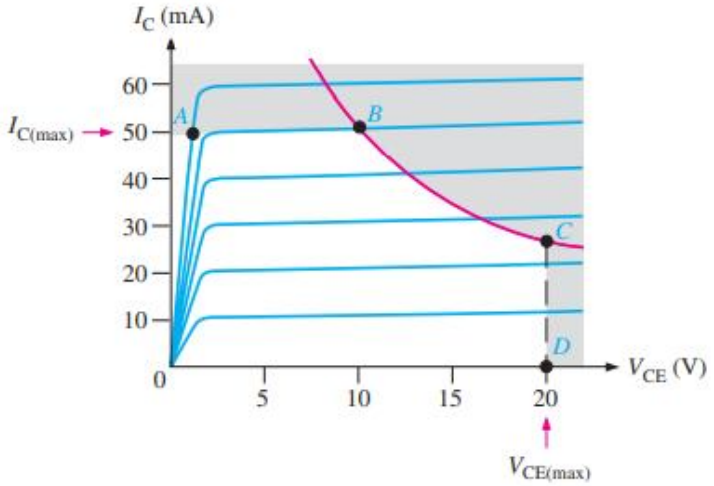
If V_{CE} ***is maximum***. I_C can be calculated as:

$$I_C = \frac{P_{D\,(max)}}{V_{CE}} \quad \dots (7A)$$

If I_C ***is maximum***, V_{CE} can be calculated by rearranging Equation above as follows:

$$V_{CE} = \frac{P_{D\,(max)}}{I_C} \quad \dots (7B)$$

For any given transistor, a maximum power dissipation curve can be plotted on the collector characteristic curves, as shown in Figure (16). These values are tabulated in this table.
Assume $P_{D\,(max)}$ is 500 mW, $V_{CE(max)}$ is 20 V, and $I_{C(max)}$ is 50 mA. The curve shows that this **particular transistor** cannot be operated **in the shaded portion of the graph**.



$P_{D(max)}$	V_{CE}	I_C
500 mW	5 V	100 mA
500 mW	10 V	50 mA
500 mW	15 V	33 mA
500 mW	20 V	25 mA

Figure (16): Maximum power dissipation curve and tabulated values.

$I_{C(max)}$ is the **limiting** rating *between* **points A and B**,
$P_{D\,(max)}$ is the **limiting** rating *between* **points B and C**, and
$V_{CE(max)}$ is the **limiting** rating *between* **points C and D**.

Example 5: A certain transistor is to be operated with $V_{CE} = 6\,V$. If its maximum power rating is $250\,mW$. What is the most collector current that it can handle?

Solution:

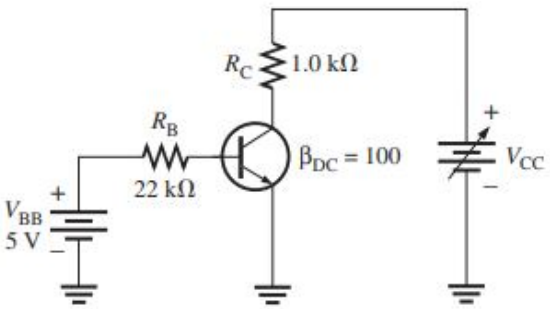
$$I_C = \frac{P_{D\,(max)}}{V_{CE}} = \frac{250 \times 10^{-3}}{6} = 41.67\,mA$$

Remember that this is not necessarily the maximum I_C. The transistor can handle more collector current if V_{CE} is reduced, as long as $P_{D\,(max)}$ is not exceeded.

H.W: Q5: If $P_{D\,(max)} = 1\,W$, how much voltage is allowed from collector to emitter if the transistor is operating with $I_C = 100\,mA$?

Solution:

Example 6: The transistor in this figure has the following maximum ratings: $P_{D(max)} = 800\,mW$, $V_{CE(max)} = 15\,V$, and $I_{C(max)} = 100\,mA$. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?



Solution:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\,V - 0.7\,V}{22\,k\Omega} = 195\,\mu A$$

$$I_C = \beta_{DC} I_B = (100)(195\,\mu A) = 19.5\,mA$$

$$V_{R_C} = I_C R_C = (19.5\,mA)(1.0\,k\Omega) = 19.5\,V$$

Now you can determine the value of V_{CC} when $V_{CE} = V_{CE(max)} = 15\,V$.

$$V_{R_C} = V_{CC} - V_{CE}$$

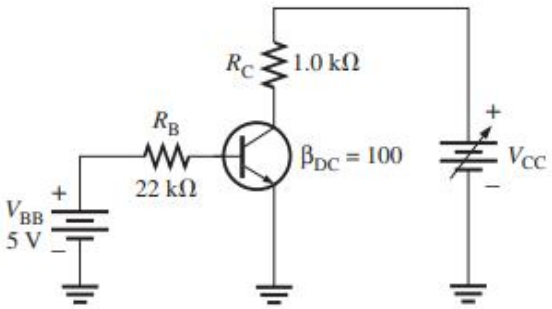
$$V_{CC(max)} = V_{CE(max)} + V_{R_C} = 15\,V + 19.5\,V = \mathbf{34.5\,V}$$

V_{CC} can be increased to 34.5 V, under the existing conditions, before $V_{CE(max)}$ is exceeded. However, at this point it is not known whether or not $P_{D(max)}$ has been exceeded.

$$P_D = V_{CE(max)} I_C = (15\,V)(19.5\,mA) = 293\,mW$$

Since $P_{D(max)}$ is 800 mW, it is not exceeded when V_{CC}=34.5 V. So, $V_{CE(max)}$=15 V is the limiting rating in this case. If the base current is removed causing the transistor to turn off, $V_{CE(max)}$ will be exceeded first because the entire supply voltage, V_{CC}, will be dropped across the transistor.

H.W: Q6: The transistor in this figure has the following maximum ratings: $P_{D(max)} = 500\,mW$, $V_{CE(max)} = 25\,V$, and $I_{C(max)} = 200\,mA$. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?



Solution:

6.12: Transistor as Two-Port Network

A **two-port network (a kind of four-terminal network or quadrupole) is an electrical network (circuit) or device with two pairs of terminals to connect to external circuits**.

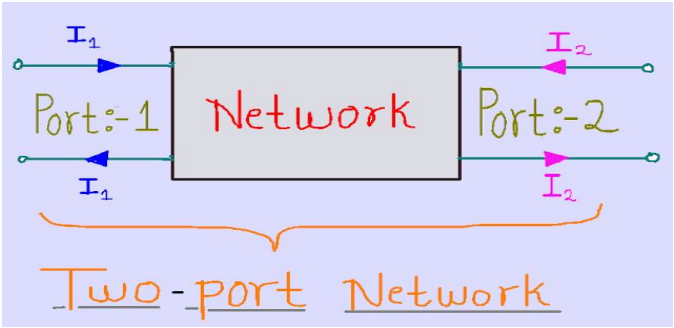


Figure (17): a: A two port network.

Two terminals constitute **a port** if the **currents applied** to them satisfy the essential requirement known as the **port condition**: the **electric current entering** one terminal must equal the **current emerging** from the other terminal on the same port but with **opposite direction**.

The ports constitute interfaces where the network connects to other networks, the points where signals are applied or outputs are taken. In a two-port network, often **port 1** is considered the **input port** and **port 2** is considered the **output port**.

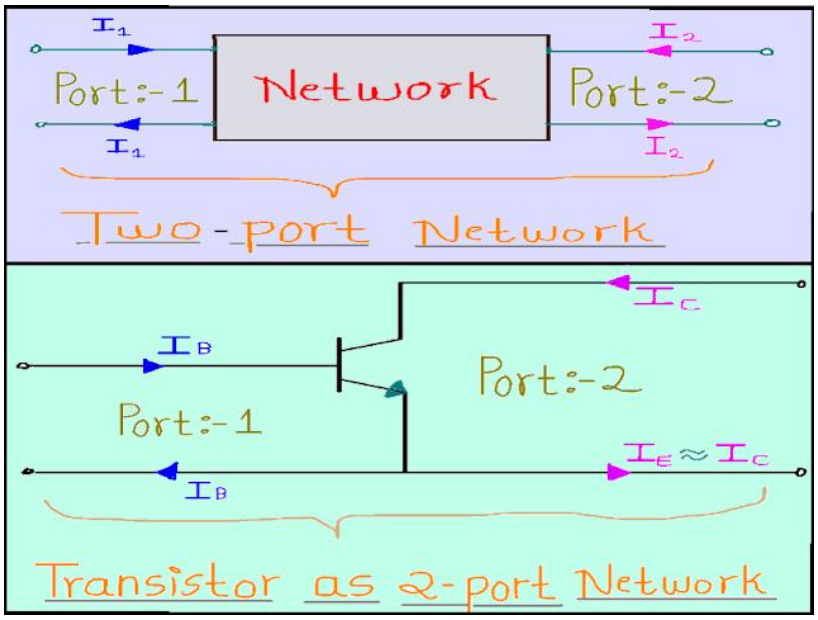


Figure (17): b: Transistor as a two-port network.

Application:

The **two-port network model** is used in mathematical circuit analysis techniques to *isolate portions* of **larger circuits**.
A **two-port network** is regarded as a "black box" *with* its properties specified by a **matrix of numbers**. This allows the response of the network to signals applied to the ports to be **calculated easily**, without solving for all the internal voltages and currents in the network. It also allows similar circuits or devices to be **compared easily**.

For example, **transistors** are often regarded as **two-ports**, characterized by their ***h-parameters*** (see below) which are listed *by the manufacturer*. Any linear circuit with four terminals can be regarded as a two-port network provided that it does not contain an independent source and satisfies the port conditions.

Examples of **circuits analyzed** as **two-ports** are ***filters***, ***mat*ching networks**, ***transmission lines***, ***transformers***, and ***small-signal models for transistors (such as the hybrid-pi model)***. The **analysis of passive two-port networks** is an outgrowth of **reciprocity theorems** first derived **by Lorentz**.

In **two-port mathematical models**, the network is described by a 2 by 2 square matrix of complex numbers.
The common models that are used are referred to as ***z-parameters***, ***y-parameters***, ***h-parameters***, ***g-parameters***, and ***ABCD-parameters***, each described individually below.

These are all limited to linear networks since an underlying assumption of their derivation is that any given circuit condition is a linear superposition of various **short-circuit** and **open-circuit conditions**. They are usually expressed in **matrix notation**, and they **establish relations** between the **variables**:
V_1 : Voltage across port 1
V_2 : Voltage across port 2
I_1 : Current into port 1
I_2 : Current into port 2
which are shown in figure (17). The difference between the various models lies in which of these variables are regarded as the independent variables. These **current** and **voltage *variables*** are most **useful** at low-to-moderate frequencies. At high frequencies (e.g., microwave frequencies), the **use** of **power** and **energy *variables*** is more appropriate, and the **two-port current–voltage** approach is replaced by an approach based upon **scattering parameters**.

6.12.1: Open Circuit Impedance Parameters (*z-Parameters*)

Figure (18): z-equivalent two port showing independent variables I_1 and I_2. Although resistors are shown, general impedances can be used instead.

The two equations of this two-port network and the corresponding ***z-parameters*** are mentioned below:

$V_1 = z_{11} \times I_1 + z_{12} \times I_2$

$V_2 = z_{21} \times I_1 + z_{22} \times I_2$

$$V = z \times I$$

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} \times \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}$$

where $z = \frac{\partial V}{\partial I}$,

$$z_{11} = z_i = \frac{\partial V_1}{\partial I_1}]_{I_2=0}\ Open\ circuit\ input\ z; \quad z_{12} = z_r = \frac{\partial V_1}{\partial I_2}]_{I_1=0}\ Open\ circuit\ revers\ transfer\ z$$

$$z_{21} = z_f = \frac{\partial V_2}{\partial I_1}]_{I_2=0}\ Open\ circuit\ forward\ transfer\ z; \quad z_{22} = z_o = \frac{\partial V_2}{\partial I_2}]_{I_1=0}\ Open\ circuit\ output\ z$$

$$\dots equation\ (8)$$

All the ***z-parameters*** have dimensions of **ohms**.

For reciprocal networks $z_{12} = z_{21}$.

For symmetrical networks $z_{11} = z_{22}$.

For reciprocal lossless networks all the z_{mn} are purely imaginary.

6.12.2: Short Circuit Admittance Parameters (y-Parameters)

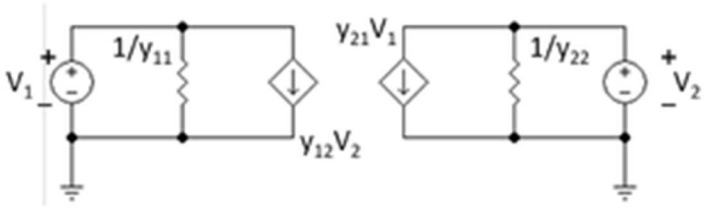


Figure (19): y-equivalent two port showing independent variables V_1 and V_2. Although resistors are shown, general admittances can be used instead.

The two equations of this two-port network and the corresponding ***y-parameters*** are mentioned below:

$I_1 = y_{11} \times V_1 + y_{12} \times V_2$

$I_2 = y_{21} \times V_1 + y_{22} \times V_2$

$$I = y \times V$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} \times \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$$

where $y = \frac{\partial I}{\partial V}$,

$$y_{11} = y_i = \frac{\partial I_1}{\partial V_1}\Big]_{V_2=0} \; Short\ circuit\ input\ y; \quad y_{12} = y_r = \frac{\partial I_1}{\partial V_2}\Big]_{V_1=0} \; Short\ circuit\ revers\ transfer\ y$$

$$y_{21} = y_f = \frac{\partial I_2}{\partial V_1}\Big]_{V_2=0} \; Short\ circuit\ forward\ transfer\ y; \quad y_{22} = y_o = \frac{\partial I_2}{\partial V_2}\Big]_{V_1=0} \; Short\ circuit\ output\ y$$

$$\ldots equation\ (9)$$

All the ***y-parameters*** have dimensions of **siemens (Ω^{-1})**.

For reciprocal networks $y_{12} = y_{21}$.

For symmetrical networks $y_{11} = y_{22}$.

For reciprocal lossless networks all the y_{mn} are purely imaginary.

6.12.3: Hybrid Parameters (h-Parameters)

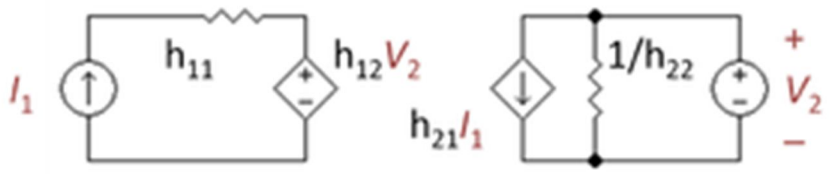


Figure (20): h-equivalent two-port showing independent variables I_1 and V_2; h_{22} is reciprocated to make a resistor.

The two equations of this two-port network and the corresponding ***h-parameters*** are mentioned below:

$V_1 = h_{11} \times I_1 + h_{12} \times V_2$

$I_2 = h_{21} \times I_1 + h_{22} \times V_2$

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \times \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}$$

where

$$h_{11} = h_i = \frac{\partial V_1}{\partial I_1}]_{V_2=0}\ Short\ circuit\ input\ z;\quad h_{12} = h_r = \frac{\partial V_1}{\partial V_2}]_{I_1=0}\ Open\ circuit\ revers\ voltage\ ratio$$

$$h_{21} = h_f = \frac{\partial I_2}{\partial I_1}]_{V_2=0}\ Short\ circuit\ forward\ current\ ratio;\quad h_{22} = h_o = \frac{\partial I_2}{\partial V_2}]_{I_1=0}\ Open\ circuit\ output\ y$$

$$\ldots equation\ (10)$$

This circuit is often selected when a current amplifier is desired at the output. The resistors shown in the diagram can be general impedances instead.

Off-diagonal ***h-parameters*** are dimensionless, while diagonal members have dimensioned the reciprocal of one another.

For reciprocal networks $h_{12} = -h_{21}$.

For symmetrical networks $h_{11}h_{22} - h_{12}h_{21} = 1$.

For reciprocal lossless networks h_{12} and h_{21} are real, while h_{11} and h_{22} are purely imaginary.

6.12.4: Inverse Hybrid Parameters (g-Parameters)

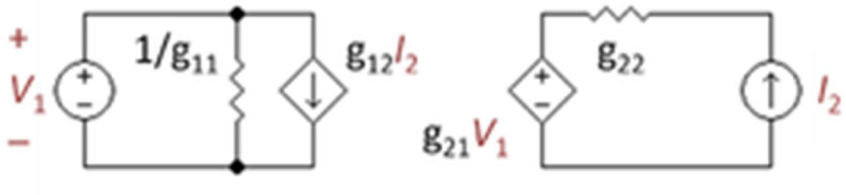


Figure (21): g-equivalent two-port showing independent variables V_1 and I_2; g_{11} is reciprocated to make a resistor.

The two equations of this two-port network and the corresponding ***g-parameters*** are mentioned below:

$I_1 = g_{11} \times V_1 + g_{12} \times I_2$

$V_2 = g_{21} \times V_1 + g_{22} \times I_2$

$$\begin{pmatrix} I_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{pmatrix} \times \begin{pmatrix} V_1 \\ I_2 \end{pmatrix}$$

where

$$g_{11} = g_i = \frac{\partial I_1}{\partial V_1}]_{I_2=0}\ Open\ circuit\ input\ y;\quad g_{12} = g_r = \frac{\partial I_1}{\partial I_2}]_{V_1=0}\ Short\ \ circuit\ revers\ current\ ratio$$

$$g_{21} = g_f = \frac{\partial V_2}{\partial V_1}]_{I_2=0}\ Open\ circuit\ forward\ voltage\ ratio;\quad g_{22} = g_o = \frac{\partial V_2}{\partial I_2}]_{V_1=0}\ \ Short\ circuit\ output\ z$$

$$\ldots equation\ (11)$$

Often this circuit is selected when a voltage amplifier is wanted at the output.

Off-diagonal ***g-parameters*** are dimensionless, while diagonal members have dimensioned the reciprocal of one another. The resistors shown in the diagram can be general impedances instead.

6.12.5: ABCD-Parameters

The two equations of this two-port network and the corresponding ***ABCD-parameters*** are mentioned below:

$V_1 = A \times V_2 - B \times I_2$

$I_1 = C \times V_2 - D \times I_2$

The ***ABCD-parameters*** are known variously as chain, cascade, or transmission parameters.

There are a number of definitions given for ***ABCD-parameters***, the most common is:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \times \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix}$$

where

$$A = \frac{\partial V_1}{\partial V_2}\Big]_{I_2=0}; \qquad B = -\frac{\partial V_1}{\partial I_2}\Big]_{V_2=0}$$

$$C = \frac{\partial I_1}{\partial V_2}\Big]_{I_2=0}; \qquad D = -\frac{\partial I_1}{\partial I_2}\Big]_{V_2=0} \quad \ldots equation\ (12)$$

For reciprocal networks $AD - BC = 1$.

For symmetrical networks $A = D$.

For networks which are reciprocal and lossless, A and D are purely real, while B and C are purely imaginary.

The two equations of this two-port network and the corresponding ***$A'B'C'D'$-parameters*** are mentioned below:

$V_2 = A' \times V_1 + B' \times I_1$

$-I_2 = C' \times V_1 + D' \times I_1$

This representation is preferred because when the parameters are used to represent a cascade of two-ports, the matrices are written in the same order that a network diagram would be drawn, that is, **left to right**. However, a variant definition is also in use:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A' & B' \\ C' & D' \end{pmatrix} \times \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix}$$

where

$$A' = \frac{\partial V_2}{\partial V_1}\Big]_{I_1=0}; \qquad B' = \frac{\partial V_2}{\partial I_1}\Big]_{V_1=0}$$

$$C' = -\frac{\partial I_2}{\partial V_1}\Big]_{I_1=0}; \qquad D' = -\frac{\partial I_2}{\partial I_1}\Big]_{V_1=0} \quad \ldots equation\ (13)$$

The negative sign of $-I_2$ arises to make the output current of one cascaded stage (as it appears in the matrix) equal to the input current of the next. Without the minus sign the two currents would have opposite senses because the positive direction of current, by convention, is taken as the current entering the port. Consequently, the input voltage/current matrix vector can be directly replaced with the matrix equation of the preceding cascaded stage to form a combined $A'B'C'D'$ matrix.

6.12.6: Scattering Parameters (*S*-Parameters)

The previous parameters are all defined in terms of voltages and currents at ports. ***S-parameters*** are different, and are defined in terms of incident and reflected waves at ports.

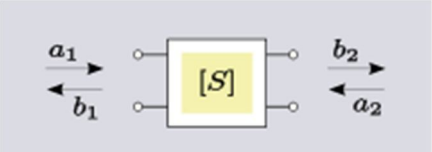


Fig.: Terminology of waves used in S-parameter definition.

S-parameters are used primarily at UHF and microwave frequencies where it becomes difficult to measure voltages and currents directly. On the other hand, incident and reflected power are easy to measure using directional couplers. The definition is:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \times \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

Where the a_k are the incident waves and the b_k are the reflected waves at port k. It is conventional to define the a_k and b_k in terms of the square root of power. Consequently, there is a relationship with the wave voltages (see main article for details).

For reciprocal networks $S_{12} = S_{21}$.
For symmetrical networks $S_{11} = S_{22}$.
For antimetrical networks $S_{11} = -S_{22}$.
For lossless reciprocal networks $|S_{11}| = |S_{22}|$ and $|S_{11}|^2 + |S_{22}|^2 = 1$.

6.12.7: Scattering transfer Parameters (*T*-Parameters)

Scattering transfer parameters, like scattering parameters, are defined in terms of incident and reflected waves. The difference is that ***T-parameters*** relate the waves at port 1 to the waves at port 2 whereas ***S-parameters*** relate the reflected waves to the incident waves. In this respect ***T-parameters*** fill the same role as ***ABCD-parameters*** and allow the ***T-parameters*** of cascaded networks to be calculated by matrix multiplication of the component networks ***T-parameters***, like ***ABCD-parameters***, can also be called transmission parameters. The definition is:

$$\begin{pmatrix} a_1 \\ b_1 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \times \begin{pmatrix} b_2 \\ a_2 \end{pmatrix}$$

T-parameters are not as easy to measure directly as ***S-parameters***.
However, ***S-parameters*** are easily converted ***to T-parameters***, see main article for details.

6.13: Determination of h-Parameters

The ***h-parameters*** can be determined graphically from the input and output characteristics of a transistor in any mode of operation.
We consider below a transistor in common emitter configuration which is most widely used mode of operation. The corresponding h-parameters are denoted by: h_ie, h_{re}, h_{fe}, and h_{oe}.

The typical input and output characteristic of a common emitter transistor are shown in figures (22) and (23). The instantaneous values of total collector voltage V_{CE}, and total collector current I_C are used in these characteristics. To determine h_{fe}, we draw a line parallel to the I_C axis figure (23) and passing through the quiescent point so as to intersect any two curves at I_{C1} and I_{C2} corresponding to the base currents I_{B1} and I_{B2} respectively. Using definition of $\boldsymbol{h_{fe}}$ as given by equation (10), we obtain:

$$h_{21} = h_f = \frac{\partial I_2}{\partial I_1}\Big]_{V_2=0} \rightarrow \boldsymbol{h_{fe}} = \frac{\partial I_C}{\partial I_B}\Big]_{V_C} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

The symbols I_C and I_B denote the instantaneous values of the output and input signal currents respectively.

Thus, substituting the values of I_{C1}, I_{C2}, I_{B1}, and I_{B2}, the parameter can be determined $\boldsymbol{h_{oe}}$. Again, from equation (10), we have:

$$h_{22} = h_o = \frac{\partial I_2}{\partial V_2}\Big]_{I_1=0} \rightarrow \boldsymbol{h_{oe}} = \frac{\partial I_C}{\partial V_C}\Big]_{I_B} \ (Slope\ of\ the\ characterstic\ curve\ at\ Q)$$

The parameters $\boldsymbol{h_{ie}}$ and $\boldsymbol{h_{re}}$ are determined from the input characteristics as shown in figure (22). The parameter hie as given by equation (10), is:

$$h_{11} = h_i = \frac{\partial V_1}{\partial I_1}\Big]_{V_2=0}$$

$$\boldsymbol{h_{ie}} = \frac{\partial V_B}{\partial I_B}\Big]_{V_{EC}} \ (Inverse\ of\ the\ slope\ of\ the\ input\ characterstic\ curve\ at\ point\ Q)$$

To determine $\boldsymbol{h_{re}}$, we draw a line parallel to V_{BE} axis and passing through the point Q, so as to intersect the curves at V_{B1} and V_{B2} corresponding to the voltages V_{C1} and V_{C2} respectively. Then using the definition of $\boldsymbol{h_{re}}$ given in equation (10), we obtain:

$$h_{12} = h_r = \frac{\partial V_1}{\partial V_2}\Big]_{I_1=0} \rightarrow \boldsymbol{h_{re}} = \frac{\partial V_B}{\partial V_C}\Big]_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

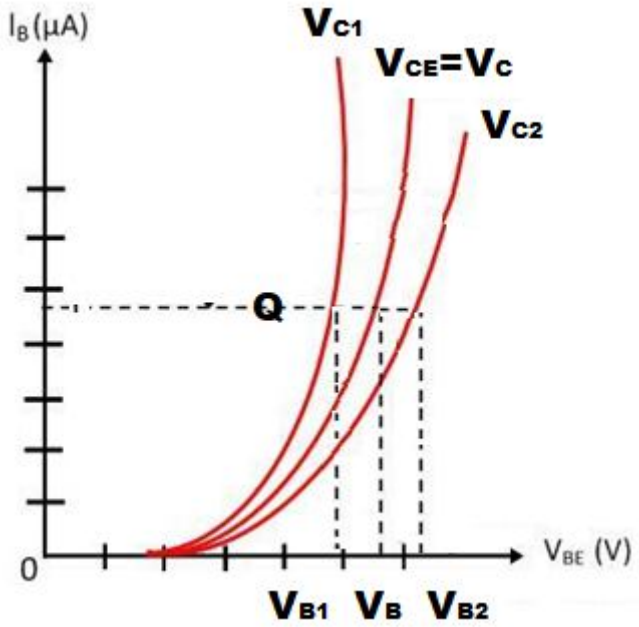


Figure (22): Typical input characteristic curves for a common emitter transistor.

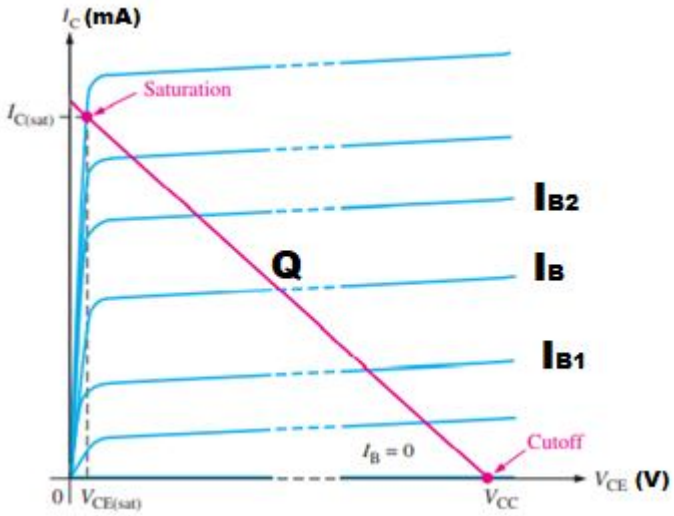


Figure (23): Typical output characteristic curves for a common emitter transistor

The ***h-parameters*** for common base and common collector configuration can be obtained in terms of the ***h-parameters*** for common emitter configuration by using the kirchoff's law and hybrid equations, and assuming that $h_{re} \ll 1$ and $h_{ie}h_{oe} \ll 1$. The results are given in table (1).

Common Emitter	Common Collector (H.W)	Common Base
$h_{ie} = \frac{\partial V_B}{\partial I_B}]_{V_{EC}}$	$h_{ic} = h_{ie}$	$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$
$h_{fe} = \frac{\partial I_C}{\partial I_B}]_{V_C} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$	$h_{fc} = -(1 + h_{fe})$	$h_{fb} = \frac{h_{fe}}{1 + h_{fe}}$
$h_{oe} = \frac{\partial I_C}{\partial V_C}]_{I_B}$	$h_{oc} = h_{oe}$	$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$
$h_{re} = \frac{\partial V_B}{\partial V_C}]_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$	$h_{rc} = 1$	$h_{rb} = \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re}$

The typical values of the three ***h-parameters*** for a junction transistor are given in table (2).

Table (2): Typical h-parameters values for a junction transistor.

Parameter	Common Emitter	Common Collector	Common Base
h_i	$1000\ \Omega$	$1000\ \Omega$	$19.6\ \Omega$
h_f	50	-51	-0.98
h_o	$25 \times 10^{-6}\ \Omega^{-1}$	$25 \times 10^{-6}\ \Omega^{-1}$	$0.49 \times 10^{-6}\ \Omega^{-1}$
h_r	2×10^{-4}	1	2.9×10^{-4}

SUMMARY:

- The BJT (bipolar junction transistor) is constructed with three regions: base, collector, and emitter.
- The BJT has two pn junctions, the base-emitter junction and the base-collector junction.
- Current in a BJT consists of both free electrons and holes, thus the term bipolar.
- The base region is very thin and lightly doped compared to the collector and emitter regions.
- The two types of bipolar junction transistor are the npn and the pnp.

- To operate as an amplifier, the base-emitter junction must be *forward-biased* and the base-collector junction must be *reverse-biased*. This is called *forward-reverse bias*.
- The three currents in the transistor are the base current (I_B), emitter current (I_E), and collector current (I_C).
- I_B is very small compared to I_C and I_E.

- The dc current gain of a transistor is the ratio of I_C to I_B and is designated β_{DC}. Values typically range from less than 20 to several hundred.
- β_{DC} is usually referred to as h_{FE} on transistor datasheets.
- The ratio of I_C to I_E is called α_{DC}. Values typically range from 0.95 to 0.99.
- There is a variation in β_{DC} over temperature and also from one transistor to another of the same type.

KEY TERMS:

Base: One of the semiconductor regions in a BJT. The base is very thin and lightly doped compared to the other regions.

Beta (β): The ratio of dc collector current to dc base current in a BJT; current gain from base to collector.

BJT: A bipolar junction transistor constructed with three doped semiconductor regions separated by two pn junctions.

Collector: The largest of the three semiconductor regions of a BJT.

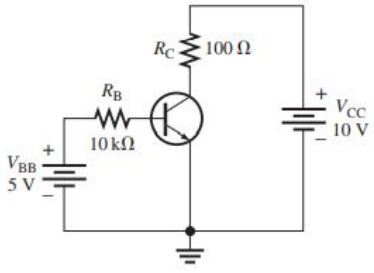
Cutoff: The nonconducting state of a transistor.

Emitter: The most heavily doped of the three semiconductor regions of a BJT.

Saturation: The state of a BJT in which the collector current has reached a maximum and is independent of the base current.

SELF-TEST: https://pinoybix.org/2019/12/self-test-in-bipolar-junction-transistors-floyd.html or https://quizlet.com/349707825/chapter-4-me327-flash-cards/

1. The three terminals of a bipolar junction transistor are called
   (a) p, n, p (b) n, p, n (c) input, output, ground (d) base, emitter, collector
2. In a pnp transistor, the p regions are
   (a) base and emitter (b) base and collector (c) emitter and collector
3. For operation as an amplifier, the base of an npn transistor must be
   (a) positive with respect to the emitter
   (b) negative with respect to the emitter
   (c) positive with respect to the collector
   (d) 0 V
4. The emitter current is always
   (a) greater than the base current (b) less than the collector current
   (c) greater than the collector current (d) answers (a) and (c)
5. The β_{DC} of a transistor is its
   (a) current gain (b) voltage gain (c) power gain (d) internal resistance
6. If I_C is 50 times larger than I_B, then β_{DC} is
   (a) 0.02 (b) 100 (c) 50 (d) 500
7. The approximate voltage across the forward-biased base-emitter junction of a silicon BJT is
   (a) 0 V (b) 0.7 V (c) 0.3 V (d) V_{BB}
8. The bias condition for a transistor to be used as a linear amplifier is called
   (a) forward-reverse (b) forward-forward (c) reverse-reverse (d) collector bias
9. If a transistor with a higher β_{DC} is used in this figure, the collector current will
   (a) increase (b) decrease (c) not change
10. If a transistor with a higher β_{DC} is used in this figure, the emitter current will
   (a) increase (b) decrease (c) not change
11. If a transistor with a higher β_{DC} is used in this figure, the base current will
   (a) increase (b) decrease (c) not change



PROBLEMS:

1. What are the majority carriers in the base region of an npn transistor called?

2. Why is the base current in a transistor so much less than the collector current?

3. What is the value of I_C for I_E = 5.34 mA and I_B = 475 mA?

4. What is the α_{DC} when I_C = 8.23 mA and I_E = 8.69 mA?

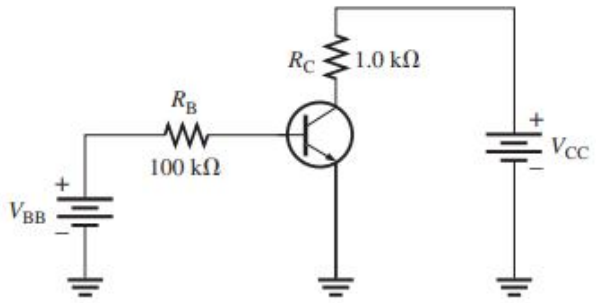
5. A certain transistor has an I_C = 25 mA and an I_B = 200 mA. Determine the β_{DC}.

6. What is the β_{DC} of a transistor if I_C = 20.3 mA and I_E = 20.5 mA?

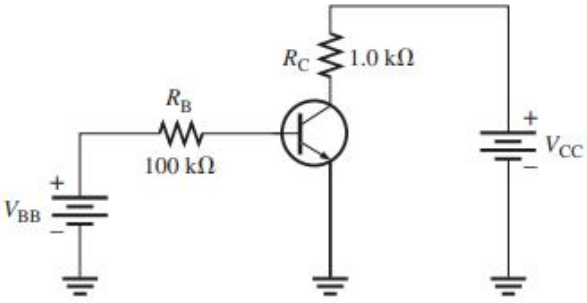
7. What is the α_{DC} if I_C = 5.35 mA and I_B = 50 mA?

8. A certain transistor exhibits an α_{DC} of 0.96. Determine I_C when I_E = 9.35 mA.

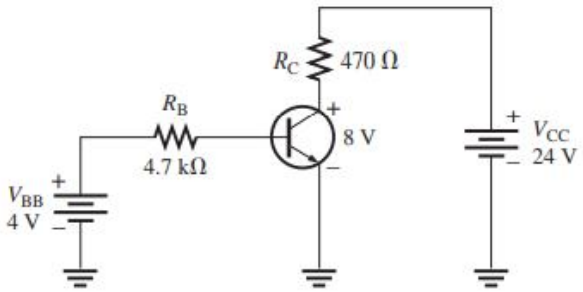
9. A base current of $50\,\mu A$ is applied to the transistor in this figure, and a voltage of $5\,V$ is dropped across R_C. Determine the β_{DC} of the transistor. Calculate α_{DC} for the transistor.



10. Assume that the transistor in the circuit of this figure is replaced with one having a β_{DC} of 200. Determine I_B, I_C, I_E, and V_{CE} given that V_{CC} = 10 V and V_{BB} = 3 V.
If V_{CC} is increased to 15 V in this figure, how much do the currents and V_{CE} change?



11. Determine each current in this figure. What is the β_{DC}?



12. Find I_B, I_E, I_C in this figure. α_{DC} = 0.98.