Chapter Eight (2nd Semester)
Field Effect Transistor (FET)

8.1: Introduction

BJTs (**Bipolar Junction Transistors**) were covered in previous chapters.
Now we will discuss the second major type of transistor, the **FET** (**Field-Effect Transistor**).
FETs are **unipolar** devices because, unlike BJTs that *use both electron and hole currents*, **they operate only with one type of charge carrier**.
The **two main types of FETs** are the **junction field-effect transistor (JFET)** and the **metal oxide semiconductor field-effect transistor (MOSFET)**.
Recall that a **BJT** is a **current-controlled device**; that is, the **base current (I_B)** *controls* the **amount of collector current (I_C)**.
A **FET** is different it is a **voltage-controlled device**, where the **voltage between two of the terminals (gate and source)** *controls* the **current through the device**.
As you will learn, a major feature of **FETs** is their **very high input resistance**.

8.2: The JFET

The **JFET** (Junction Field-Effect Transistor) is a type of **FET** that **operates with a reverse-biased** $p-n$ junction to control the **current in a channel**. Depending on their structure, JFETs fall into either of two categories, ***n*-channel** or ***p*-channel**.

After completing this section, you should be able to:

- ❑ Explain the operation of JFETs
- ❑ Identify the three terminals of a JFET
- ❑ Explain what a channel is
- ❑ Describe the structural difference between an n-channel JFET and a p-channel JFET
- ❑ Discuss how voltage controls the current in a JFET
- ❑ Identify the symbols for n-channel and p-channel JFETs

8.2.1: JFET Symbols

The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in Figure (8.1). Notice that the arrow on the gate points "**in" for *n*-channel** and **"out" for *p*-channel**.

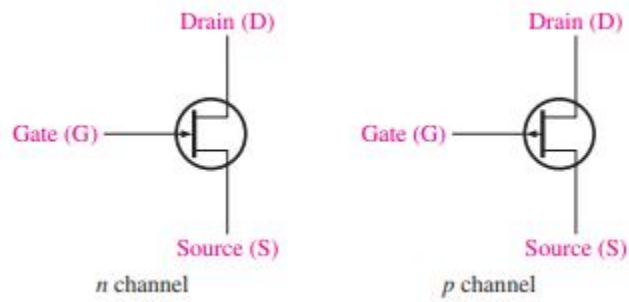


Figure (8.1): JFET schematic symbols.

8.2.2: Basic Structure

Figure (8.2a) shows the basic structure of an ***n*-channel JFET**.
Wire leads are *connected* to each end of the ***n*-channel**; the **drain is at the upper end**, and the **source is at the lower end**.
Two *p*-type regions are *diffused in* the ***n*-type** material to *form (create)* **a channel**, and **both *p*-type regions** are *connected* to the **gate lead**.
For simplicity, the **gate lead** is shown as *connected to* **only one of the *p* regions**.
A *p*-channel JFET is shown in Figure (8.2b).

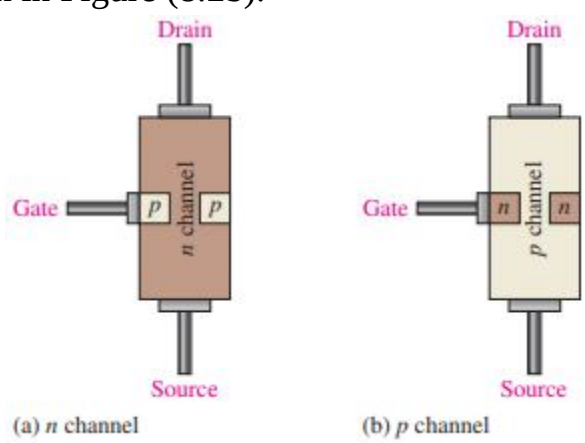


Figure (8.2): A representation of the basic structure of the two types of JFET.

8.2.3: Basic Operation

To illustrate the operation of a JFET, Figure (8.3) shows ***dc* bias voltages** *applied to* an ***n*-channel** device.
V_{DD} provides a **drain-to-source voltage** and supplies **current from drain to source** (I_D).
V_{GG} sets the **reverse-bias voltage** *between* **the gate and the source**, as shown.

The **JFET** is **always operated** *with* the **gate-source *pn* junction reverse-biased**.
Reverse biasing of the gate-source junction *with* a negative gate voltage *produces* a depletion region along the *pn* junction, which *extends into* the *n*-channel and *thus* **increases its resistance** by restricting the **channel width**.

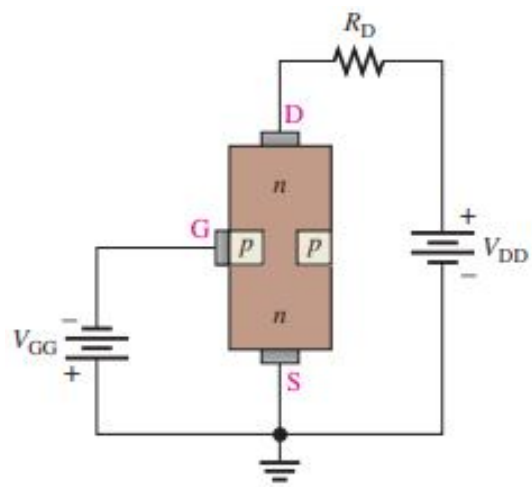
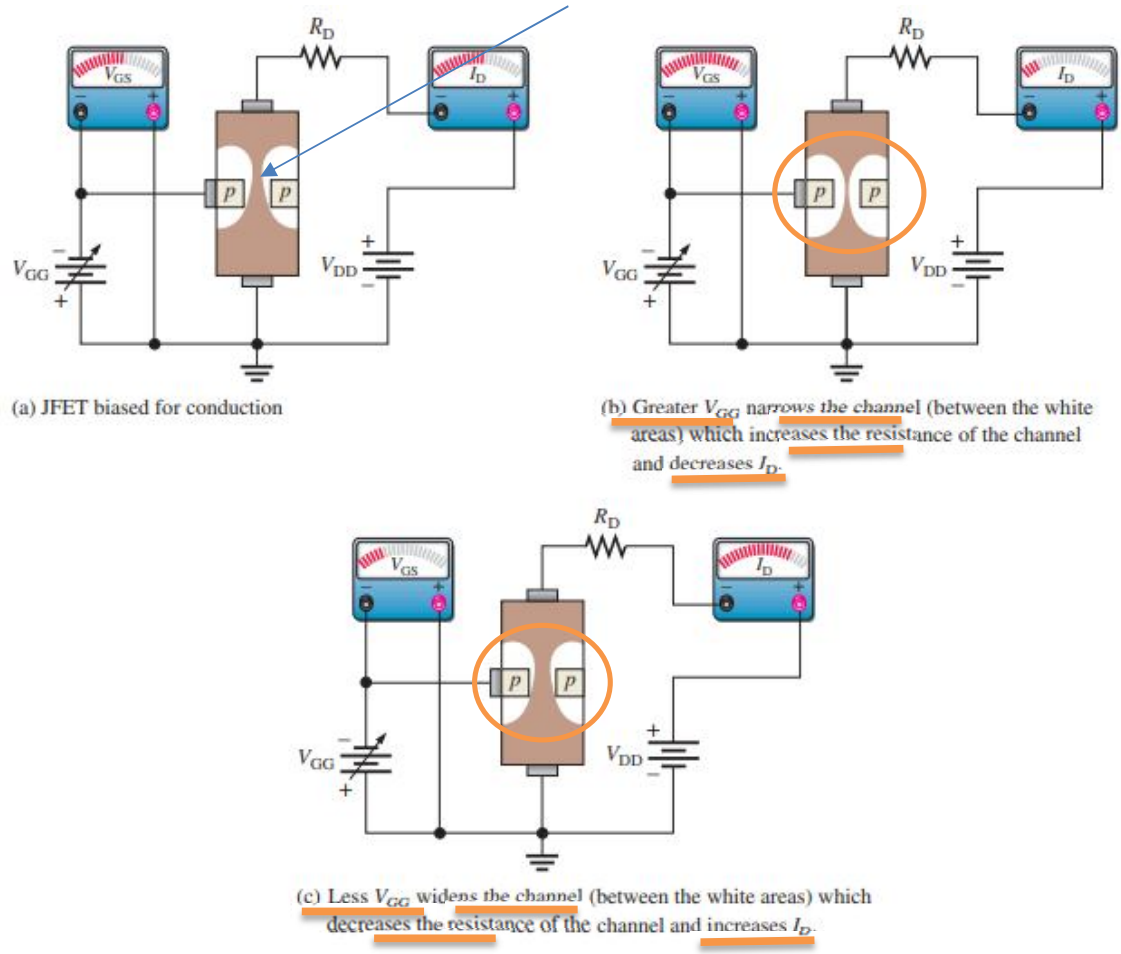


Figure (8.3): A biased *n*-channel JFET.

The **channel width** and thus the **channel resistance** *can be controlled* by **varying the gate voltage**. Thereby *controlling* the amount of **drain current** (I_D).

Figure (8.4) illustrates this concept.
The **white areas** *represent* the **depletion region** *created by* the **reverse bias**.
It is **wider** toward the **drain end** of the channel *because* the **reverse-bias voltage between the gate and the drain** is **greater than** that **between the gate and the source**.

We will discuss JFET **characteristic curves** and **some important parameters** in Section 8.3.



(a) JFET biased for conduction

(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.

(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

Figure (8.4): Effects of V_{GS} on channel width, resistance, and drain current ($V_{GG} = V_{GS}$).

8.3: JEFT Characteristics and Parameters

In this section, you will **see how the JFET operates as a voltage-controlled**, constant- current device. You will also learn about **cutoff** and **pinch-off** as well as JFET transfer characteristics.

After completing this section, you should be able to:

- ❑ Define, discuss, and apply important JFET parameters
- ❑ Explain ohmic area, constant-current area, and breakdown
- ❑ Define pinch-off voltage
- ❑ Describe how gate-to-source voltage controls the drain current
- ❑ Define cutoff voltage
- ❑ Compare pinch-off and cutoff
- ❑ Analyze a JFET transfer characteristic curve

- ❑ Use the equation for the transfer characteristic to calculate I_D
- ❑ Use a JFET data sheet
- ❑ Define transconductance
- ❑ Explain and determine input resistance and capacitance
- ❑ Determine drain-to-source resistance

8.3.1: Drain Characteristic Curve

Consider the case when the gate-to-source voltage is zero ($\boldsymbol{V_{GS} = 0\ V}$). This is produced by shorting the gate to the source, as in Figure (8.5a) where both are grounded.
As $\boldsymbol{V_{DD}}$ (and thus $\boldsymbol{V_{DS}}$) is **increased from $\boldsymbol{0\ V}$**, $\boldsymbol{I_D}$ will **increase** proportionally, as shown in the graph of Figure (8.5b) **between points A and B**. In this area, the channel **resistance is essentially constant** because the depletion region is not large enough to have a significant effect. This is called the **ohmic area** because V_{DS} and I_D are related by Ohm's law.

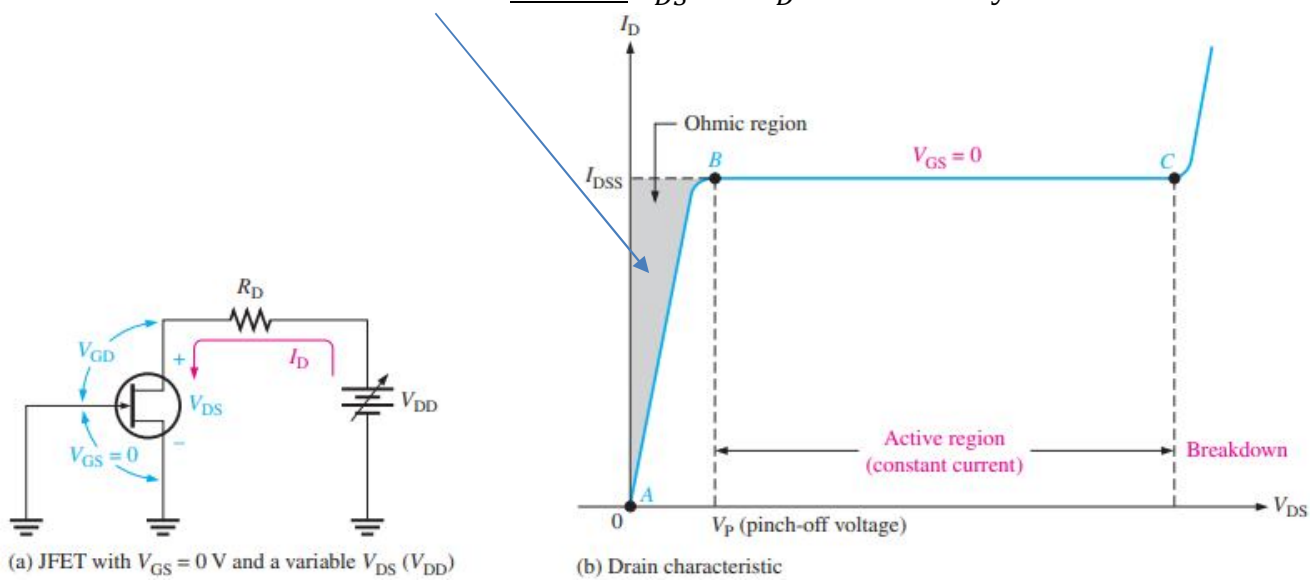


Figure (8.5): The drain characteristic curve of a JFET for $\boldsymbol{V_{GS} = 0}$ showing pinch-off.

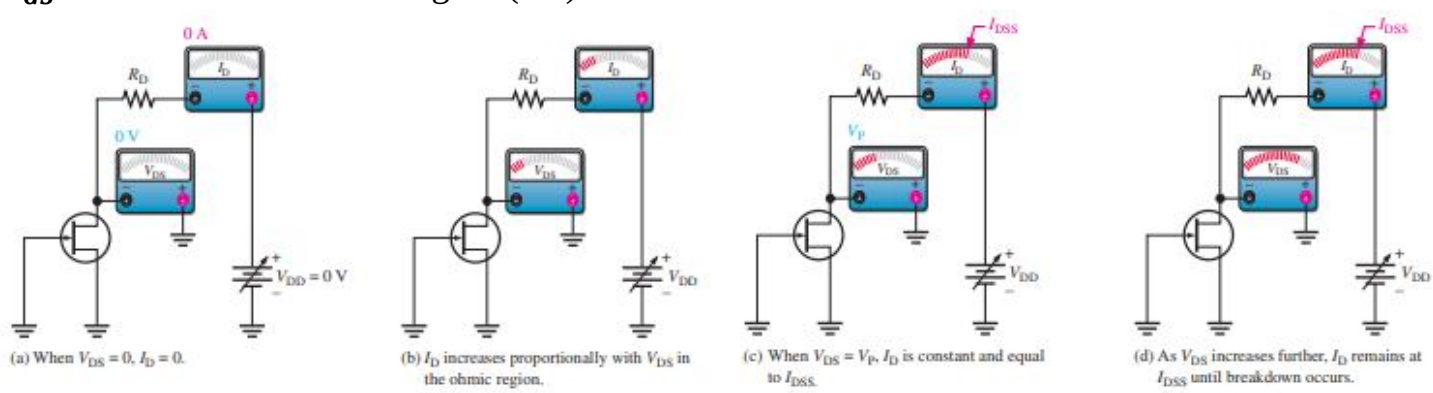
At point B in Figure (8.5b), the curve levels off and $\boldsymbol{I_D}$ becomes essentially **constant**.
As $\boldsymbol{V_{DS}}$ **increases from point B to point C**, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping $\boldsymbol{I_D}$ **relatively constant**.

8.3.2: Pinch-Off Voltage (V_P)

For $V_{GS} = 0\ V$, the value of V_{DS} at which I_D becomes essentially constant (**point B on the curve** in Figure (8.5b)) **is the pinch-off voltage V_P**.
For a given JFET, **V_P has a fixed value**. As you can see, a **continued increase in V_{DS}** above the **pinch-off voltage** produces an **almost constant drain current**.
This value of **drain current I_D is I_{DSS}** (**Drain to Source current with gate Shorted**) and *is always specified* ***on JFET data sheets***. **I_{DSS} is the maximum drain current** that a specific JFET can produce regardless of the external circuit, and it is always specified **for the condition $V_{GS} = 0\ V$**.

8.3.3: Breakdown

As shown in the graph in Figure (8.5b), **breakdown occurs at point C** when **I_D begins to increase very rapidly** with any further **increase in V_{DS}**. **Breakdown** can result in **irreversible (don't back) damage to the device**, so **JFETs** are always operated **below breakdown**, and **within the constant-current area** (between points B and C on the graph).
The JFET action that produces the drain characteristic curve to the point of **breakdown for $V_{GS} = 0\ V$** is illustrated in Figure (8.6).



(a) When $V_{DS} = 0$, $I_D = 0$.
(b) I_D increases proportionally with V_{DS} in the ohmic region.
(c) When $V_{DS} = V_P$, I_D is constant and equal to I_{DSS}.
(d) As V_{DS} increases further, I_D remains at I_{DSS} until breakdown occurs.

Figure (8.6): JFET action that produces the characteristic curve for $V_{GS} = 0$.

8.3.4: V_{GS} Controls I_D

Let's connect a bias voltage V_{GG}, from gate to source as shown in Figure (8.7a).
As V_{GS} is **set to increase more negative values** by adjusting V_{GG}, a family of **drain characteristic curves is produced**, as shown in Figure (8.7b).

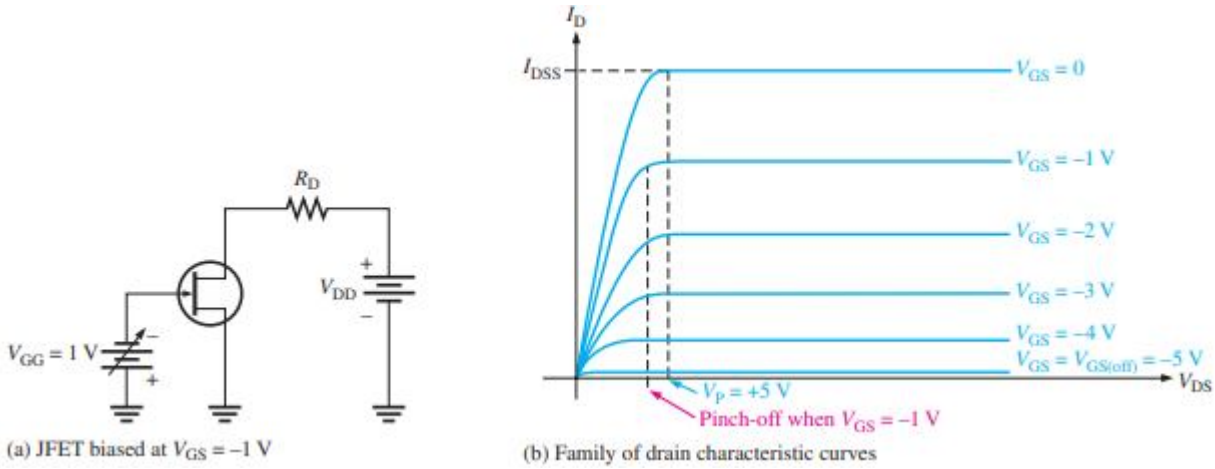


Figure (8.7): Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.

Notice that **I_D decreases as the magnitude of V_{GS} are increased to larger negative values because of the narrowing of the channel**. Also notice that, **for each increase in V_{GS}**, the **JFET reaches pinch-off** (where constant current begins) at values of **V_{DS} less than V_P**. Therefore, the **amount of drain current is controlled by V_{GS}**, as illustrated in Figure (8.8).

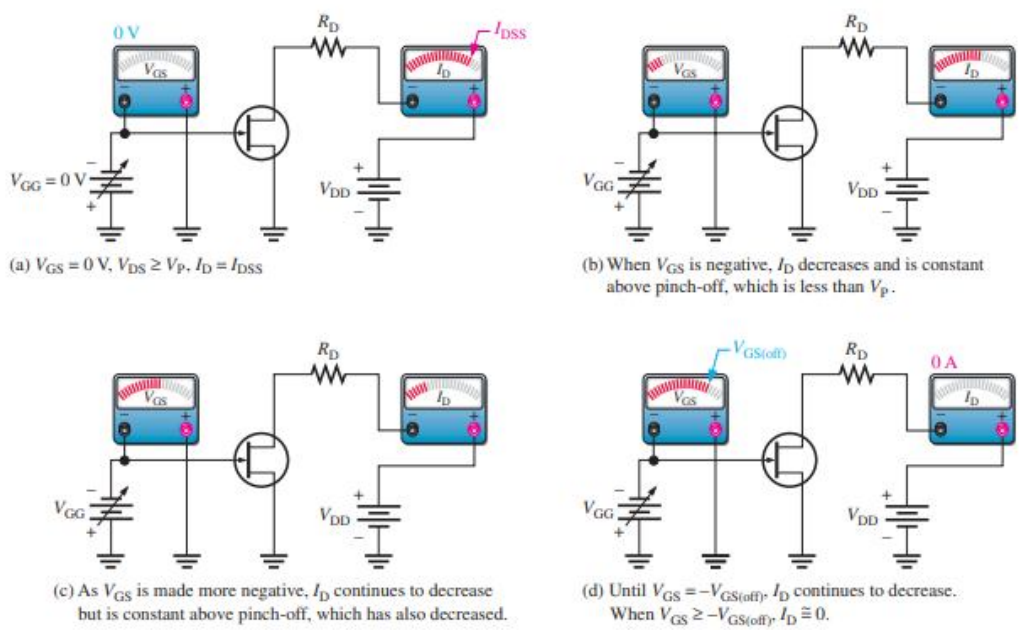


Figure (8.8): V_{GS} controls I_D.

8.3.5: Cutoff Voltage ($V_{GS\,(off)}$)

The **value of V_{GS} that makes I_D approximately zero** is the **cutoff voltage $V_{GS\,(off)}$**, as shown in Figure (8.8d).

The **JFET** must be operated between $V_{GS} = 0\ V$ **and** $V_{GS\,(off)}$.

For this range of gate-to-source voltages, **I_D will vary from a maximum of I_{DSS} to a minimum of almost zero**.

As you have seen, **for an n-channel JFET**, the **more negative V_{GS} is the smaller I_D** becomes in *the constant-current area*.

When **V_{GS} has a sufficiently large negative value**, **I_D is reduced to zero**.

This cutoff effect is caused by the widening of the depletion region to a point where it completely doses the channel, as shown in Figure (8.9).

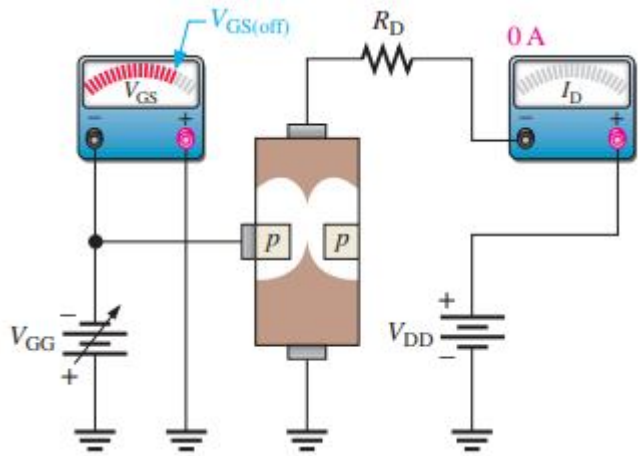


Figure (8.9): JFET at cutoff.

The basic **operation of a p-channel JFET** is the same as **for an n-channel device** except that a p-channel JFET requires a **negative V_{DD}** and a **positive V_{GS}**, as illustrated in Figure (8.10).

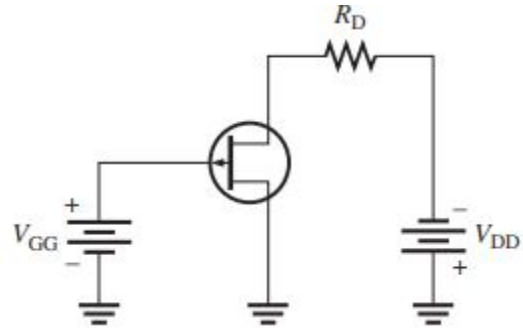
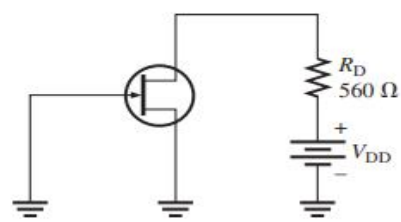


Figure (8.10): A biased p-channel JFET.

8.3.6: Comparison of Pinch-Off Voltage and Cutoff Voltage

As you have seen, there is a **difference between pinch-off and cutoff**.
There is also a connection; $\boldsymbol{V_P}$ **is the value of** $\boldsymbol{V_{DS}}$ at which the drain current $\boldsymbol{I_D}$ **becomes constant** and **is always measured at** $\boldsymbol{V_{GS} = 0\ V}$.
However, **pinch-off** occurs **for** $\boldsymbol{V_{DS}}$ **values less than** $\boldsymbol{V_P}$ when $\boldsymbol{V_{GS}}$ **is nonzero**.
So, although $\boldsymbol{V_P}$ **is a constant**, the **minimum value of** $\boldsymbol{V_{DS}}$ at which $\boldsymbol{I_D}$ **becomes constant varies with** $\boldsymbol{V_{GS}}$. $\boldsymbol{V_{GS\,(off)}}$ **and** $\boldsymbol{V_P}$ **are always equal in magnitude but opposite in sign**.
A datasheet usually will give **either** $\boldsymbol{V_{GS\,(off)}}$ or $\boldsymbol{V_P}$, **but not both**.
However, *when you know one, you have the other*.
For example, **if** $\boldsymbol{V_{GS\,(off)} = -5\ V}$. **then** $\boldsymbol{V_P = +5\ V}$. as shown in Figure (8.7b).

Example 1: For the JFET in this figure, $V_{GS\,(off)} = -4\ V$ and $I_{DSS} = 12\ mA$. Determine the minimum value of V_{DD} required to put the device in the constant current area of operation.



Solution:

Since $V_{GS(off)} = -4$ V, $V_P = 4$ V. The minimum value of V_{DS} for the JFET to be in its constant-current region is

$$V_{DS} = V_P = 4\text{ V}$$

In the constant-current region with $V_{GS} = 0$ V,

$$I_D = I_{DSS} = 12\text{ mA}$$

The drop across the drain resistor is

$$V_{R_D} = I_D R_D = (12\text{ mA})(560\ \Omega) = 6.72\text{ V}$$

Apply Kirchhoff's law around the drain circuit.

$$V_{DD} = V_{DS} + V_{R_D} = 4\text{ V} + 6.72\text{ V} = \mathbf{10.7\ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

H.W: Q1: If V_{DD} is increased to 15 V, what is the drain current?
Solution:

Example 2: A particular p-channel JFET has a $V_{GS\,(off)} = +4\,V$ What is I_D when $V_{GS} = +6\,V$?

Solution:

The p-channel JFET requires a positive gate-to-source voltage. The more positive the voltage, the less the drain current. When V_{GS} = 4 V, I_D=0. Any further increase in V_{GS} keeps the JFET cut off, so I_D remains 0.

8.3.7: JFET Transfer Characteristic

You have learned that a **range of V_{GS} values from zero to $V_{GS\,(off)}$** controls the amount of drain current I_D.

For an n-channel JFET, **$V_{GS\,(off)}$ is negative**, and for a p-channel JFET, **$V_{GS\,(off)}$ is positive**. Because V_{GS} does control I_D the relationship between these two quantities is *very important*. Figure (8.11) is a general transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D. This curve is also known as a **transconductance curve**.

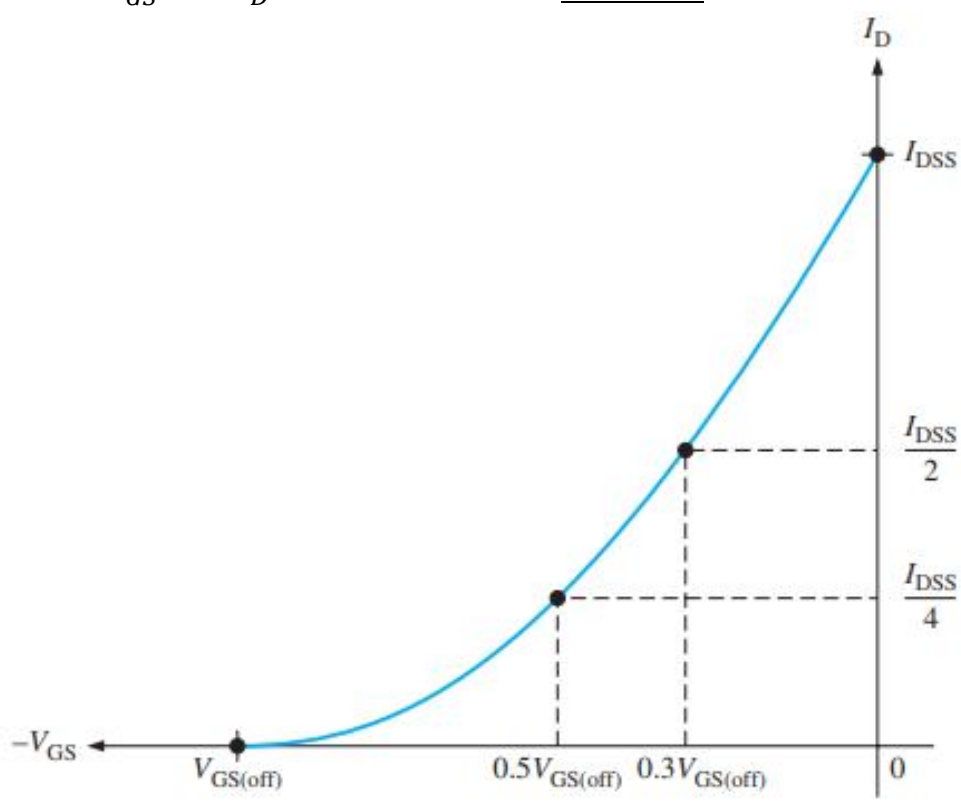


Figure (8.11): JFET transfer characteristic curve (n-channel).

Notice that the bottom end of the curve is at a point on the **V_{GS} axis equal to $V_{GS\,(off)}$**, and the top end of the curve is at a point on the **I_D axis equal to I_{DSS}**.

This curve shows that:

$$I_D = 0 \quad when\ V_{GS} = V_{GS\,(off)}$$

$$I_D = \frac{I_{DSS}}{4} \quad when\ V_{GS} = 0.5\ V_{GS\,(off)}$$

$$I_D = \frac{I_{DSS}}{2} \quad when\ V_{GS} = 0.3\ V_{GS\,(off)}$$

and $$I_D = I_{DSS} \quad when\ V_{GS} = 0$$

The transfer characteristic curve can be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch off, as illustrated in Figure (8.12) for a specific set of curves.

Each point on the transfer characteristic curve corresponds to specific values of V_{GS} and I_D on the drain curves.

For example, **when** $V_{GS} = -2\ V$, $I_D = 4.32\ mA$. Also, for this specific JFET, $V_{GS\,(off)} = -5\ V$ and $I_{DSS} = 12\ mA$.

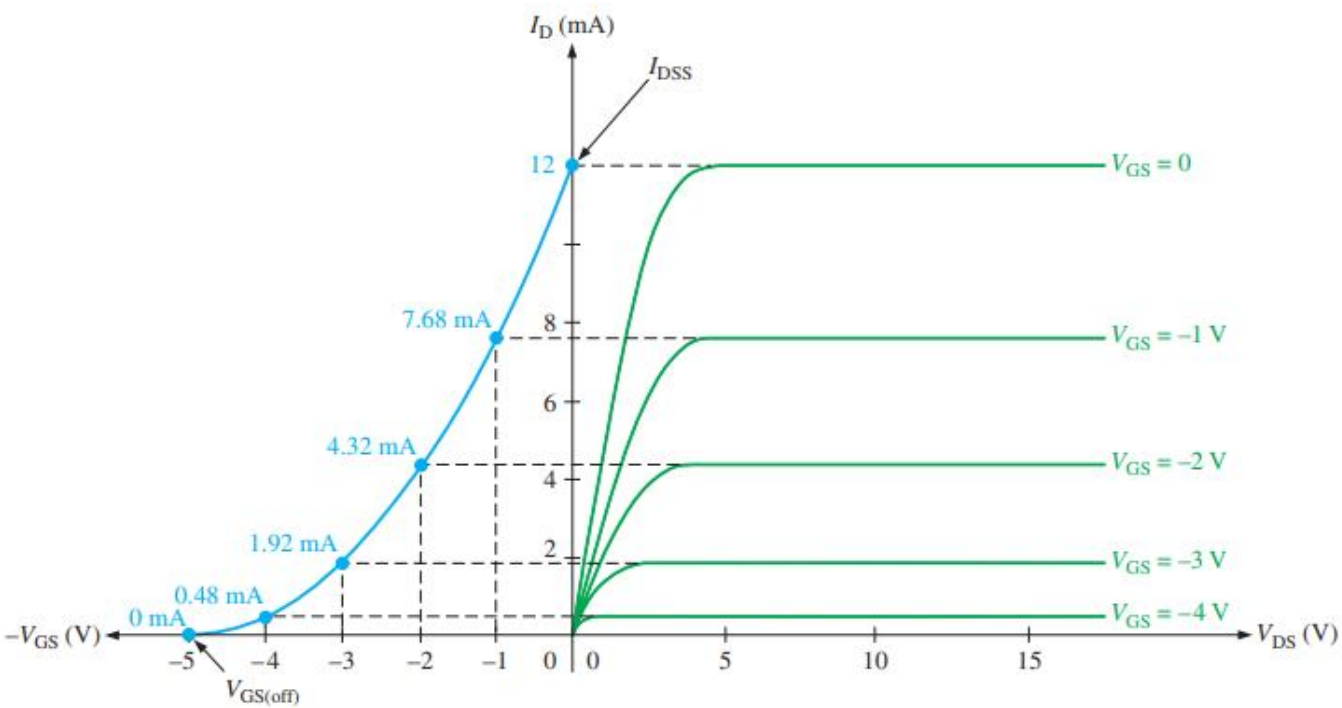


Figure (8.12): Example of the development of an n-channel FET transfer characteristic curve (blue) from the FET drain characteristic curves (green).

A **JFET transfer characteristic curve** is expressed as:

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 \quad \ldots (1)$$

With Equation (1), **I_D can be determined for any V_{GS} if $V_{GS\,(off)}$ and I_{DSS} are known**. These quantities are usually available from the data sheet for a given JFET.

Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a square law and therefore, **JFETs** and **MOSFETs** are often referred to as square-law devices.

Example 3: The partial data sheet for a 2N5459 JFET indicates that typically $I_{DSS} = 9\,mA$ and $V_{GS\,(off)} = -8\,V$ (maximum). Using these values. determine the drain current for $V_{GS} = 0\,V, -1\,V$ and $-4\,V$.

Solution:

For $V_{GS} = 0$ V,

$$I_D = I_{DSS} = \mathbf{9\ mA}$$

For $V_{GS} = -1$ V

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$
$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = \mathbf{6.89\ mA}$$

For $V_{GS} = -4$ V,

$$I_D \cong (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = \mathbf{2.25\ mA}$$

H.W: Q2: Determine I_D for $V_{GS} = -3\,V$ for the 2N5459 JFET.

Solution:

8.3.8: JFET Forward Transconductance (g_m)

The **forward transconductance** (**transfer conductance**) (g_m) **is the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage constant**. It is expressed as a ratio and has the unit of **siemens (S)** (Ω^{-1}).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \; at \; constant \; V_{DS}$$

Other common designations for this parameter are g_{fs} and y_{fs} (**forward transfer admittance**). **g_m is important in FET amplifiers as a major factor in determining the voltage gain**.

Because the t**ransfer characteristic curve for a JFET is nonlinear**. g_m varies in value depending on **the location on the curve as set by V_{GS}**.
The value for g_m is **greater near the top of the curve (near $V_{GS} = 0$)** than it is **near the bottom (near $V_{GS\,(off)}$** as illustrated in Figure (8.13).

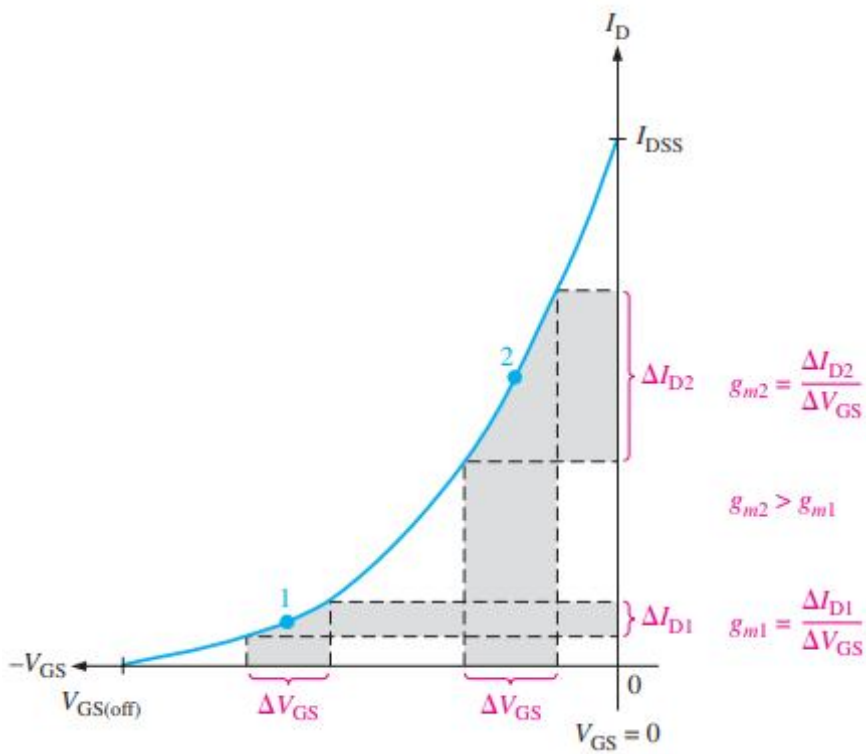


Figure (8.13): g_m varies depending on the bias point (V_{GS}).

A data sheet normally gives the value of gm measured at $V_{GS} = 0\,V$ (g_{m0}). For example, the data sheet for the 2N5457 JFET specifies a minimum g_{m0} (g_{fs}) of $1000\,S$ with $V_{DS} - 15\,V$.

Given g_{m0}, you can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following formula:

$$g_m \cong g_{m0}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right) \quad \dots (2)$$

When a value of g_{m0} is not available, you can calculate it using values of I_{DSS} and $V_{GS\,(off)}$ the vertical lines indicate an absolute value (no sign).

$$g_{m0} = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|} \quad \dots (3)$$

Example 4: The following information is included on the data sheet for a 2N5457 JFET: typically. $I_{DSS} = 3\,mA$. $V_{GS\,(off)} = -6\,V$ maximum, and $g_{fs(max)} = 5000\,\mu s$. Using these values, determine the forward transconductance for $V_{GS} = -4\,V$, and find I_D at this point.

Solution:

$g_{m0} = g_{fs} = 5000\,\mu S$. Use Equation 2 to calculate g_m

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = (5000\,\mu S)\left(1 - \frac{-4\,V}{-6\,V}\right) = \mathbf{1667\,\mu S}$$

Next, use Equation 1 to calculate I_D at $V_{GS} = -4\,V$.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (3.0\,mA)\left(1 - \frac{-4\,V}{-6\,V}\right)^2 = \mathbf{333\,\mu A}$$

H.W: Q3: A given JFET has the following characteristics: $I_{DSS} = 12\,mA$. $V_{GS\,(off)} = -5\,V$, and $g_{m0} = 3000\,\mu s$. Find gill and I_D when $V_{GS} = -2\,V$.

Solution:

8.3.9: Input Resistance and Capacitance

As you know, a JFET operates with its gate-source junction reverse-biased which makes the input resistance at the gate very high. This high input resistance is one advantage of the JFET over the BJT. (*Recall that a bipolar junction transistor operates with a forward-biased base-emitter junction.*) JFET data sheets often specify the input resistance by giving a value for the **gate reverse current I_{GSS}** at a certain gate-to-source voltage. The **input resistance** can then be determined using the following equation, where the vertical lines indicate an absolute value (no sign):

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

For example, **the 2N5457 data sheet in a maximum I_{GSS} of 1.0 nA for $V_{GS} = -15\,V$ at 25°C. I_{GSS} increases with temperature, so the input resistance decreases**.

The **input capacitance C_{iss}** is a result of the JFET operating with a **reverse-biased pn junction**.

Recall that a **reverse-biased pn junction acts as a capacitor** whose **capacitance** depends on **the amount of reverse voltage**. For example, **the 2N5457 has a maximum C_{iss} of $7pF$ for $V_{GS} = 0$**.

Example 5: A certain JFET has an I_{GSS} of $-2\,nA$ for $V_{GS} = -20\,V$. Detennine the input resistance.

Solution:

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{20\text{ V}}{2\text{ nA}} = \mathbf{10{,}000\ M\Omega}$$

8.3.10: AC Drain-to-Source Resistance

You learned from the drain characteristic curve that, above pinch-off, the drain current is relatively constant over a range of drain-to-source voltages. Therefore, a **large change in V_{DS}** produces only a **very small change in I_D**. The **ratio of these changes** is the **drain-to-source resistance of the device, r'_{ds}**:

$$r'_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

Data sheets often specify this parameter in terms of the **output conductance g_{os}**, or **output admittance y_{os}**.

SECTION 8.3 REVIEW:

1. The drain-to-source voltage at the pinch-off point of a particular JFET is 7V. If the gate-to-source voltage is zero, what is V_p?
2. The V_{GS} of a certain n-channel JFET is increased negatively. Does the drain current increase or decrease?
3. What value must V_{GS} have to produce cutoff in a p-channel JFET with a $V_p = -3\,V$?

8.4: JFET Biasing

Using some of the FET parameters discussed in the previous sections, you will now see how to dc-bias JFETs. Just as with the BJT, the purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and thus a proper $Q-point$. **You will learn about two types of bias circuits, self-bias and voltage-divider bias**.

After completing this section, you should be able to:

- ❑ Discuss and analyze JFET bias circuits
- ❑ Describe self-bias
- ❑ Analyze a self-biased JFET circuit
- ❑ Set the self-biased $Q-point$
- ❑ Analyze a JFET circuit with voltage-divider bias
- ❑ Use transfer characteristic curves to analyze JFET bias circuits
- ❑ Discuss $Q-point$ stability

8.4.1: Self-Bias

Self-bias is the most common type of JFET bias.

Recall that a JFET must be operated such that the gate-source junction is always **reverse-biased**. This condition requires a **negative V_{GS}** for an **n-channel JFET** and a **positive V_{GS}** for a **p-channel JFET**. This can be achieved using the self-bias arrangements shown in Figure (8.14).

The **gate resistor R_G, does not affect the bias** because it has essentially **no voltage drop** across it; and therefore, the **gate remains at 0V**.

R_G is necessary only to isolate an ac signal from ground in amplifier applications. as you will see later.

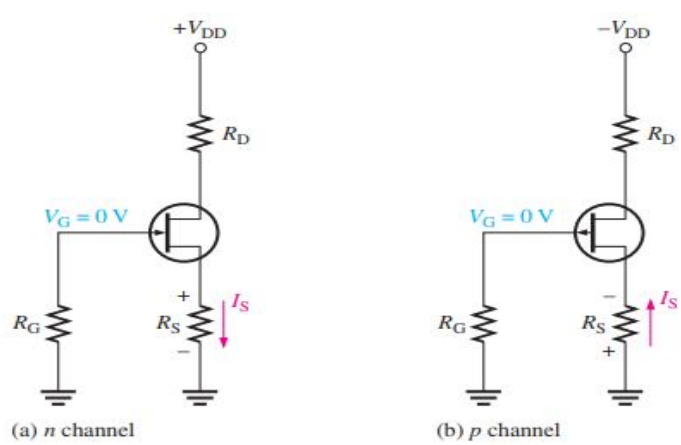


Figure (8.14): Self-biased JFETs ($I_S = I_D$ in all FETs).

For the n-channel JFET in Figure (8.14a), **the current I_S produces a voltage drop across R_s and makes the source positive with respect to ground**, Since $I_S = I_D$ and $V_G = 0$, then: $V_S = I_D R_s$
The **gate-to-source voltage** is: $V_{GS} = V_G - V_S = 0 - I_D R_s = -I_D R_s$
Thus:

$$V_{GS} = -I_D R_s$$

For the p-channel JFET shown in Figure (8.14b), **the current I_S through R_s produces a negative voltage at the source**, making the gate positive with respect to the source.
Therefore, since:

$$I_S = I_D \quad and \quad V_{GS} = +I_D R_s$$

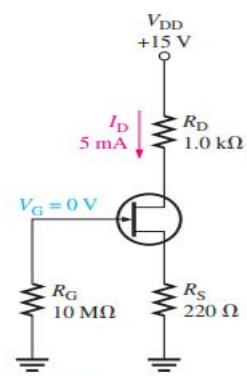
In the following analysis, the n-channel JFET in Figure (8.14a) is used for illustration. Keep in mind that analysis of the p-channel JFET is the same except for opposite-polarity voltages.
The **drain voltage with respect to ground** is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

Since $V_S = I_D R_s$, the **drain-to-source voltage** is:

$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_s)$$

Example 6: Find V_{DS} and V_{GS} in this figure. For the particular JFET in this circuit, the internal parameter values such as g_m, $V_{GS(off)}$, and I_{DSS} are such that a drain current (I_D) of approximately 5 mA is produced. Another JFET, even of the same type. may not produce the same results when connected in this circuit due to the variations in parameter values.



Solution:

$$V_S = I_D R_S = (5\text{ mA})(220\ \Omega) = 1.1\text{ V}$$
$$V_D = V_{DD} - I_D R_D = 15\text{ V} - (5\text{ mA})(1.0\text{ k}\Omega) = 15\text{ V} - 5\text{ V} = 10\text{ V}$$

Therefore,

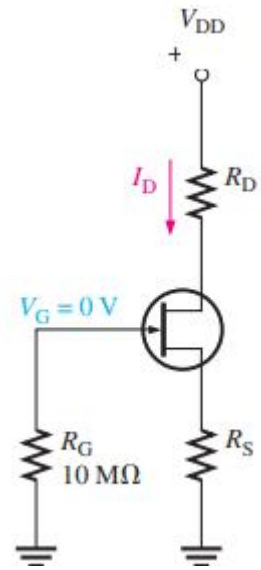
$$V_{DS} = V_D - V_S = 10\text{ V} - 1.1\text{ V} = \mathbf{8.9\text{ V}}$$

Since $V_G = 0$ V,

$$V_{GS} = V_G - V_S = 0\text{ V} - 1.1\text{ V} = \mathbf{-1.1\text{ V}}$$

H.W: Q4: Determine V_{DS} and V_{GS} in this figure when $I_D = 8\,mA$. Assume that $R_D = 860\,\Omega$, $R_S = 390\Omega$, and $V_{DD} = 12\,V$.

Solution:



Setting the $Q - Point$ of a Self-Biased JFET:

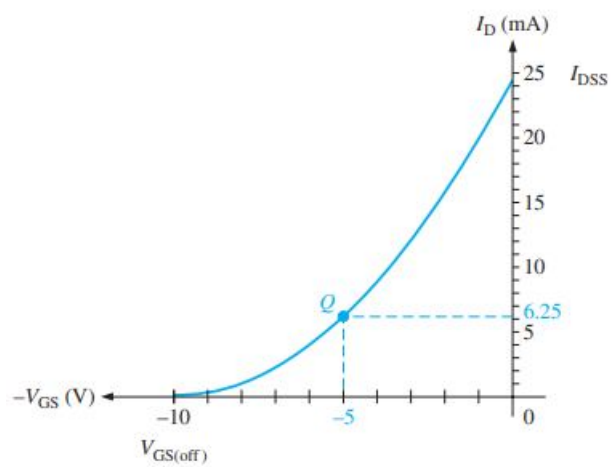
Then **calculate the required value of R_S using the following relation-ship**. The vertical lines indicate an absolute value.

$$R_S = \left|\frac{V_{GS}}{I_D}\right|$$

Example 7: Determine the value of R_S required to self-bias an n-channel JFET that has the transfer characteristic curve shown in this figure at $V_{GS} = -5\,V$.

Solution:

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = R_S = \left|\frac{-5}{6.25 \times 10^{-3}}\right| = 800\Omega$$



Example 8: Determine the value of R_S required to self-bias a p-channel JFET with datasheet values of $I_{DSS} = 25\,mA$ and $V_{GS(off)} = 15\,V$. V_{GS} is to be 5 V.

Solution:

Use Equation (1) to calculate I_D.

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (25\text{ mA})\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2$$
$$= (25\text{ mA})(1 - 0.333)^2 = 11.1\text{ mA}$$

Now, determine R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5\text{ V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$$

H.W: Q5: Find the value of R_S required to self-bias a p-channel JFET with $I_{DSS} = 18\,mA$ and $V_{GS(off)} = 8\,V$. $V_{GS} = 4\,V$.

Solution:

8.4.2: Voltage-Divider Bias

An n-$channel$ JFET with voltage-divider bias is shown in Figure (8.15). The **voltage at the source** of the JFET must be more **positive** than the **voltage at the gate** in order to keep the **gate-source junction reverse-biased**.

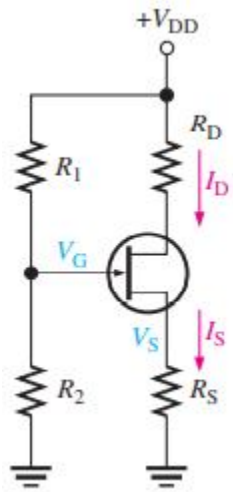


Figure (8.15): An n-channel JFET with voltage divider bias ($I_s = I_D$).

The **source voltage** is: $V_S = I_D R_S$

The **gate voltage** is set by resistors R_1 and R_2 as expressed by the following equation using the voltage-divider formula:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

The **gate-to-source voltage** is: $V_{GS} = V_G - V_S$

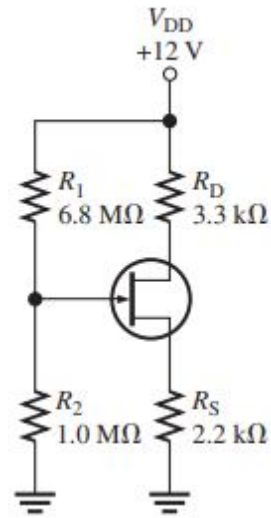
and the **source voltage** is: $V_S = V_G - V_{GS}$

The drain current can be expressed as: $I_D = \frac{V_S}{R_S}$

Substituting for V_S:

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

Example 9: Determine I_D and V_{GS} for the JFET with voltage-divider bias in this figure, given that for this particular JFET the internal parameter values are such that $V_D \cong 7\,V$.



Solution:

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = \mathbf{1.52\text{ mA}}$$

Calculate the gate-to-source voltage as follows:

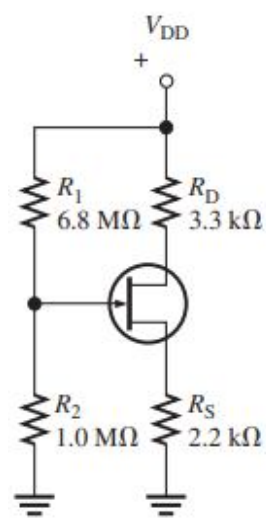
$$V_S = I_D R_S = (1.52\text{ mA})(2.2\text{ k}\Omega) = 3.34\text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{1.0\text{ M}\Omega}{7.8\text{ M}\Omega}\right)12\text{ V} = 1.54\text{ V}$$

$$V_{GS} = V_G - V_S = 1.54\text{ V} - 3.34\text{ V} = \mathbf{-1.8\text{ V}}$$

If V_D had not been given in this example the $Q - point$ values could not have been found without the transfer characteristic curve.

H.W: Q6: Given that $V_D = 6\,V$ when another JFET is inserted in the circuit of this figure, determine the $Q - point$.



Solution:

SECTION 8-3 REVIEW:

1. Should a p-channel JFET have a positive or a negative V_{GS}?
2. In a certain self-biased n-$channel$ JFET circuit, $I_D = 8\,mA$ and $R_S = 1.0\,k\Omega$. Determine V_{GS}.
3. An n-channel JFET with voltage-divider bias has a gate voltage of $3\,V$ and a source voltage of $5\,V$. Calculate V_{GS}.

8.5: THE MOSFET

The **MOSFET** (**Metal Oxide Semiconductor Field-Effect Transistor**) is **another** category of **field-effect transistor**.
The **MOSFET** differs from the **JFET** in that it **has no pn junction structure**; instead, **the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer**.
The **two basic types of MOSFETs** are **depletion (D)** and **enhancement (E)**. Because of the insulated gate, these devices are sometimes called **IGFETs** (**insulated-gate FETs**).

After completing this section, you should be able to:

❑ Explain the operation of MOSFETs

❑ Describe the structural difference between an n-channel and a p-channel depletion MOSFET (D-MOSFET)

❑ Explain the depletion mode

❑ Explain the enhancement mode

❑ Identify the symbols for n-channel and p-channel D-MOSFETs

❑ Describe the structural difference between an n-channel and a p-channel enhancement MOSFET (E-MOSFET)

❑ Identify the symbols for n-channel and p-channel E-MOSFETs

❑ Explain how D-MOSFETs and E-MOSFETs differ

❑ Discuss power MOSFETs

❑ Discuss dual-gate MOSFETs

8.5.1: Depletion MOSFET (D-MOSFET)

One type of MOSFET is the **depletion MOSFET (D-MOSFET)**, and Figure (8.16) illustrates its basic structure. The **drain and source** are **diffused into the substrate material** and **then connected by a narrow channel adjacent to the insulated gate**. Both *n*-channel and *p*-channel devices are shown in the figure.
We will use the ***n*-channel device** to describe the **basic operation**.
The ***p*-channel operation** is the **same**, except the **voltage polarities are opposite those of the *n*-channel**.

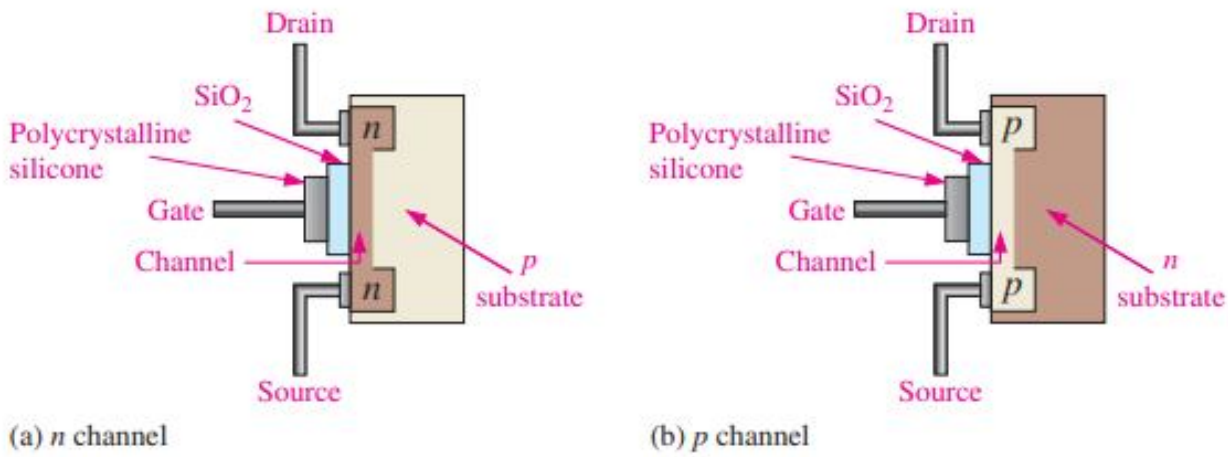


Figure (8.16): Representation of tile basic structure of D-MOSFETs.

The **D-MOSFET** can be operated in either of **two modes-the depletion mode** or **the enhancement mode**−and is **sometimes called** a **depletion/enhancement MOSFET**. Since the gate is insulated from the channel. either a positive or a negative gate voltage can be applied.
The ***n*-channel MOSFET operates in the depletion mode** when a **negative** gate-to-source voltage is applied and in the **enhancement mode** when a **positive** gate-to-source voltage is applied. **These devices are generally operated in the depletion mode**.

Depletion Mode:

Visualize the **gate as one plate of a parallel-plate capacitor** and the **channel as the other plate**. The **silicon dioxide insulating layer** is the dielectric.
With a negative gate voltage, the **negative charges on the gate** repel **conduction electrons from the channel**, **leaving positive ions in their place**. Thereby, the ***n*-channel is depleted**

of some of its electrons, thus **decreasing the channel conductivity**. The **greater the negative voltage on the gate**, the **greater the depletion of n-channel electrons**.
At a sufficiently negative gate-to-source voltage $V_{GS(off)}$, the **channel is totally depleted** and the **drain current is zero**. This **depletion mode is illustrated in Figure (8.17a)**. Like the n-channel JFET, the n-channel D-MOSFET conducts **drain current** for gate-to-source voltages between $\boldsymbol{V_{GS(off)}}$ **and zero**. In addition, the D-MOSFET conducts for values of $\boldsymbol{V_{GS}}$ **above zero**.

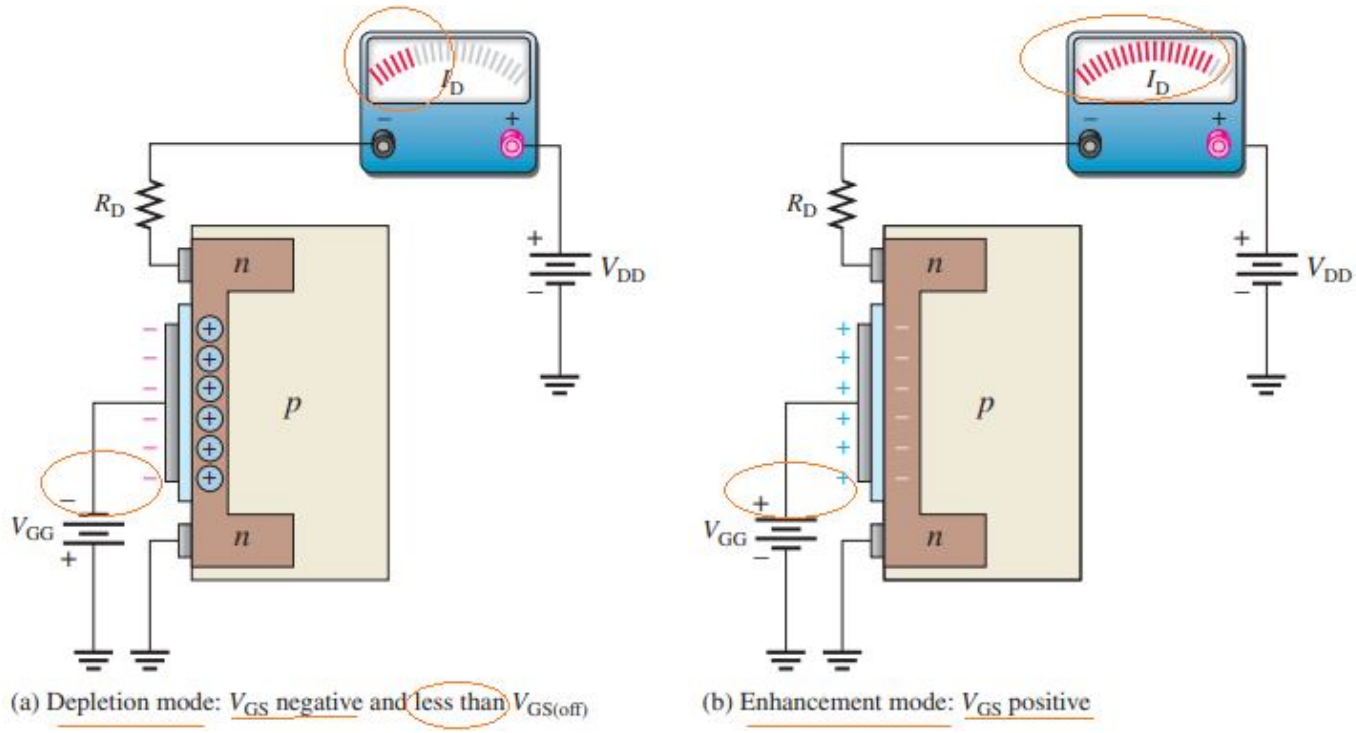


Figure (8.17): Operation of n-channel D-MOSFET.

Enhancement Mode:

With a **positive gate voltage**, more **conduction electrons are attracted into the channel**, thus **increasing (enhancing) the channel conductivity**, as illustrated in Figure (8.17b).

D-MOSFET Symbols:

The schematic symbols for both the n-channel and the p-channel depletion MOSFETs are shown in Figure (8.18). The substrate, indicated by the arrow, is normally (but not always) connected internally to the source. Sometimes, there is a separate substrate pin. An **inward-pointing substrate arrow** is **for n-channel**, and an **outward-pointing arrow** is **for p-channel**.

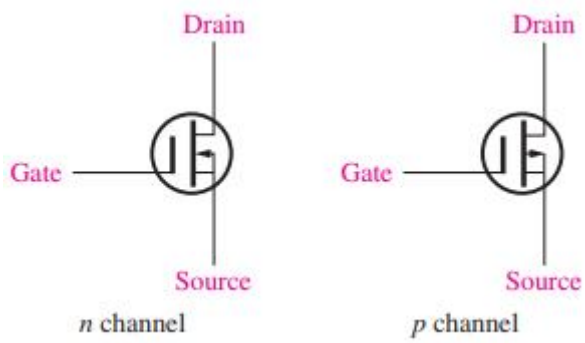


Figure (8.18): D-MOSFET schematic symbols.

8.5.2: Enhancement MOSFET (E-MOSFET)

The **E-MOSFET** operates only in the **enhancement mode** and **has no depletion mode**.
It differs in construction from the D-MOSFET in that it **has no structural channel**.
Notice in Figure (8.19a) that the substrate extends completely to the Sio_2 layer.
For an n-channel device, a **positive gate voltage above a threshold value** induces **a channel by creating a thin layer of negative charges** in the substrate region adjacent to the Sio_2 layer. as shown in Figure (8.19b).
The **conductivity of the channel is enhanced** by **increasing the gate-to-source voltage** and thus **pulling more electrons** into the channel area.
For any gate voltage below the threshold value, **there is no channel**.

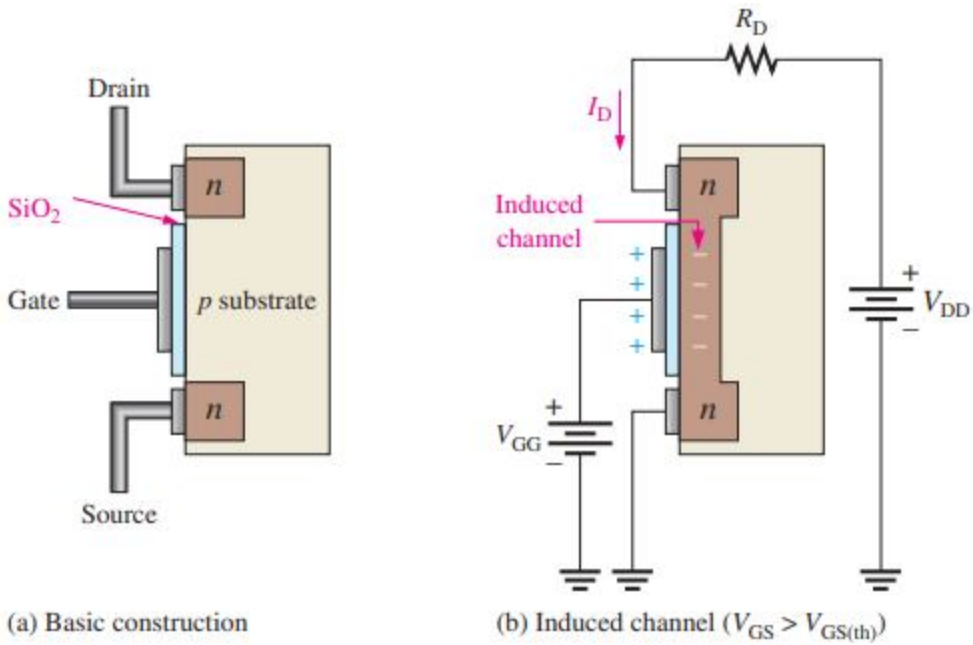


Figure (8.19): Representation of the basic E-MOSFET construction and operation (n-channel).

E-MOSFET Symbols:

The schematic symbols for the n-$channel$ and p-channel E-MOSFETs are shown in Figure (8.20). The **broken lines symbolize the** absence **of a physical channel**. Like the D-MOSFET, some devices have a separate substrate connection.

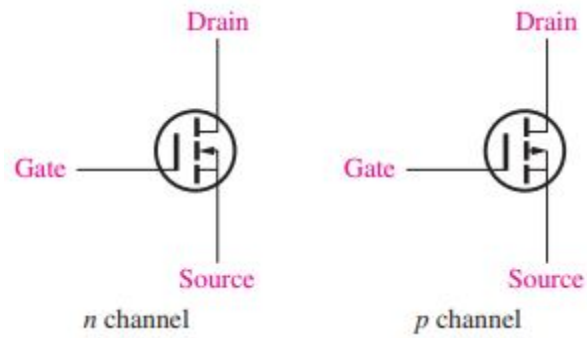


Figure (8.20): E-MOSFET schematic symbols.

8.6: MOSFET Characteristics and Parameters

Much of the discussion concerning JFET **characteristics and parameters apply** equally to MOSFETs. In this section, MOSFET parameters are discussed.

After completing this section. you should be able to:

❑ Define, discuss, and apply important MOSFET parameters

❑ Analyze a D-MOSFET transfer characteristic curve Use the equation for the D-MOSFET transfer characteristic to calculate I_D

❑ Analyze an E-MOSFET transfer characteristic curve

❑ Use the equation for the E-MOSFET transfer characteristic to calculate I_D

❑ Use a MOSFET data sheet

❑ Discuss handling precautions for MOS device

8.6.1: D-MOSFET Transfer Characteristic

As previously discussed, the **D-MOSFET** can operate with either **positive** or **negative gate voltages**. This is indicated on the general transfer characteristic curves in Figure (8.21) for both n-channel and p-channel MOSFETs. The point on the curves where $\boldsymbol{V_{GS} = 0}$ corresponds to $\boldsymbol{I_{DSS}}$.

The point where $\boldsymbol{I_D = 0}$ corresponds to $\boldsymbol{V_{GS(off)}}$ As with the JFET, $\boldsymbol{V_{GS(off)} = -V_P}$. The square-law expression in Equation (1) for the JFET curve also applies to the D-MOSFET curve, as Example 10 demonstrates.

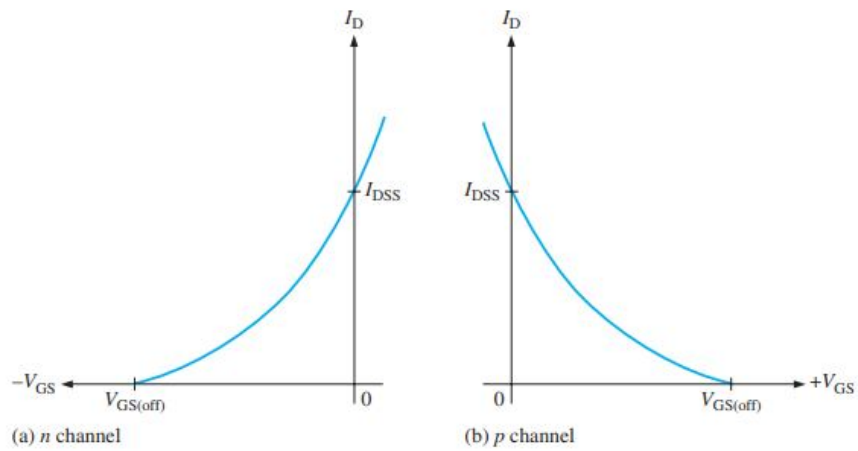


Figure (8.21): D-MOSFET general transfer characteristic curves.

Example 10: For a certain D-MOSFET, $I_{DSS} = 10\,mA$ and $V_{GS(off)} = -8\,V$. (a) I_S this an n-channel or a p-channel? (b) Calculate I_D at $V_{GS} = -3\,v$. (c) Calculate I_D at $V_{GS} = +3\,V$.

Solution:

(a) The device has a negative $V_{GS(off)}$; therefore, it is an ***n*-channel** MOSFET.

(b) $I_D \cong I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\text{ mA})\left(1 - \dfrac{-3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{3.91\text{ mA}}$

(c) $I_D \cong (10\text{ mA})\left(1 - \dfrac{+3\text{ V}}{-8\text{ V}}\right)^2 = \mathbf{18.9\text{ mA}}$

H.W: Q7: For a certain D-MOSFET, $I_{DSS} = 18\,mA$ and $V_{GS(off)} = +10\,V$. (a) I_S this an n-channel or a p-channel? (b) Determine I_D at $V_{GS} = +4\,V$. (c) Determine I_D at $V_{GS} = -4\,V$.

Solution:

8.6.2: E-MOSFET Transfer Characteristic

The **E-MOSFET** uses only **channel enhancement**. Therefore, an ***n*-channel device** requires *a positive gate-to-source voltage*, and a ***p*-channel device** requires *a negative gate-to-source voltage*. Figure (8.22) shows the general transfer characteristic curves for both types of E-MOSFETs.

As you can see, **there is no drain current when $V_{GS} = 0$**. Therefore, the **E-MOSFET does not have a significant I_{DSS} parameter**, as do the JFET and the D-MOSFET.

Notice also that there is ideally **no drain current until V_{GS}** reaches a certain nonzero value called the **threshold voltage $V_{GS(th)}$**.

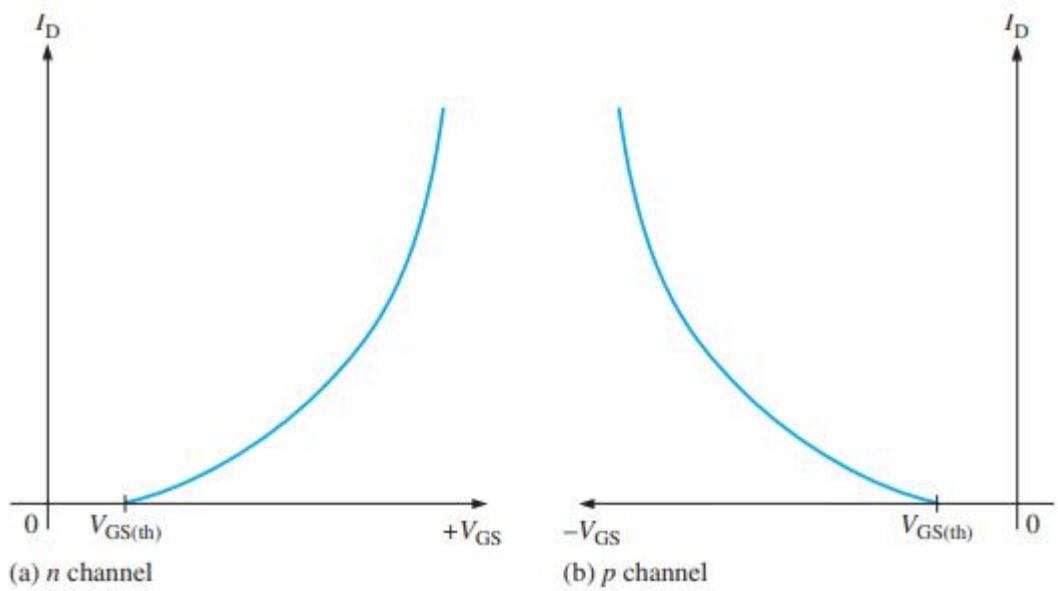


Figure (8.22): E-MOSFET general transfer characteristic curves.

The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at $V_{GS(th)}$ **rather than** $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The **equation for the E-MOSFET transfer characteristic curve** is:

$$I_D = K(V_{GS} - V_{GS(th)})^2 \quad \text{... (4)}$$

The **constant *K*** **depends on** the **particular MOSFET** and can be determined from the **data sheet** by taking the specified value of I_D **called** $I_{D(on)}$, at the given value of V_{GS} and substituting the values into Equation (4). A typical E-MOSFET data sheet is given in Figure (8.23).

Example 11: The data sheet for a 2N7008 E-MOSFET gives $I_{D(on)} = 500\,mA$ (minimum) at $V_{GS} = 10V$ and $V_{GS(th)} = 1\,V$. Determine the drain current for $V_{GS} = 5\,V$.

Solution:

First, solve for K using Equation 4.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

H.W: Q8: The data sheet for an E-MOSFET gives $I_{D(on)} = 100\,mA$ at $V_{GS} = 8\,V$ and $V_{GS(th)} = 4\,V$. Find I_D when $V_{GS} = 6\,V$.

Solution:

8.7: MOSFET Biasing

Three ways to bias a MOSFET are zero-bias, voltage-divider bias, and drain-feedback bias. Biasing is important in FET amplifiers which you will study in the next chapter.

After completing this section, you should be able to:

- ❑ Discuss and analyze MOSFET bias circuits
- ❑ Describe zero-bias of a D-MOSFET
- ❑ Analyze a zero-biased MOSFET circuit
- ❑ Describe voltage-divider bias of an E-MOSFET
- ❑ Describe drain-feedback bias of an E-MOSFET

8.7.1: D-MOSFET Bias

Recall that **D-MOSFETs** can be operated with either **positive** or **negative values of V_{GS}**.
A simple bias method is to set $V_{GS} = 0$ so that an ac signal at the gate varies the gate-to-source voltage above and below this $0V$ bias point. **A MOSFET with zero bias is shown in Figure (8.23a)**.

Since $V_{GS} = 0$, $I_D = I_{DSS}$ as indicated. The **drain-to-source voltage** is expressed as follows:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

The **purpose of R_G is to accommodate an ac signal input by isolating it from the ground**, shown in Figure (8.23b). Since **there is no dc gate current**. **R_G does not affect the zero gate-to-source bias**.

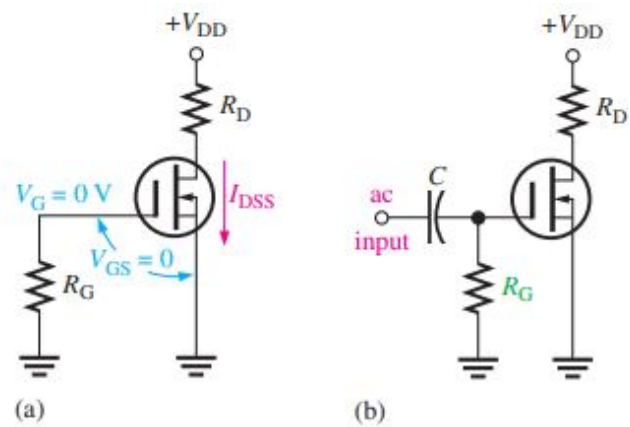
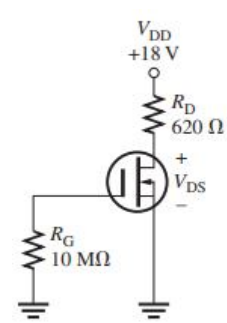


Figure (8.23): A zero-biased D-MOSFET.

Example 12: Determine the drain-to-source voltage in the circuit of this figure. The MOSFET data sheet gives $V_{GS(oft)} = -8V$ and $I_{DSS} = 12\ mA$.



Solution:

Since $I_D = I_{DSS} = 12$ mA, the drain-to-source voltage is

$$V_{DS} = V_{DD} - I_{DSS}R_D = 18\text{ V} - (12\text{ mA})(620\ \Omega) = \mathbf{10.6\ V}$$

H.W: Q9: Find V_{DS} in this figure when $V_{GS(oft)} = -10V$ and $I_{DSS} = 20\ mA$.

Solution:

8.7.2: E-MOSFET Bias

Recall that E-MOSFETs must have **a V_{GS} greater than the threshold value $V_{GS(th)}$, so zero bias cannot be used**. **Figure (8.24) shows two ways to bias an E-MOSFET** (D-MOSFETs can also be biased using these methods).

An n-channel device is used for purposes of illustration.

In either the voltage-divider or drain-feedback bias arrangement, the purpose is to make **the gate voltage more positive than the source** by an amount exceeding $V_{GS(th)}$ **Equations** for the analysis of the voltage-divider bias in Figure (8.24a) are as follows:

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

$$V_{DS} = V_{DD} - I_D R_D$$

where $I_D = K(V_{GS} - V_{GS(th)})^2$ from Equation (4).

In the drain-feedback bias circuit in Figure (8.24b), **there is negligible gate current** and, therefore, **no voltage drop across R_G** This makes $V_{GS} = V_{DS}$.

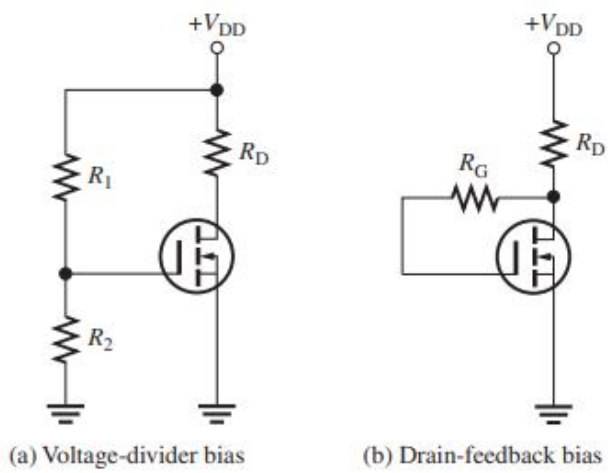
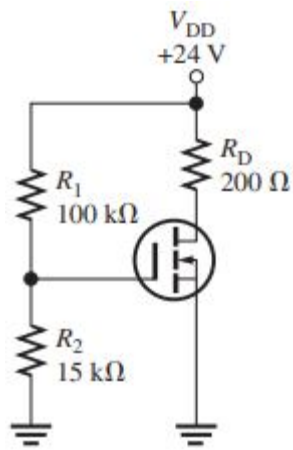


Figure (8.24): Common E-MOSFET biasing arrangements.

Example 13: Determine V_{GS} and V_{DS} for the E-MOSFET circuit in this figure. Assume this particular MOSFET has minimum values of $I_{D(ON)} = 200\ mA$ at $V_{GS} = 4\ V$ and $V_{GS(th)} = 2\ V$.



Solution:

For the E-MOSFET in Figure , the gate-to-source voltage is

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\ k\Omega}{115\ k\Omega}\right)24\ V = \mathbf{3.13\ V}$$

To determine V_{DS}, first find K using the minimum value of $I_{D(on)}$ and the specified voltage values.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\ mA}{(4\ V - 2\ V)^2} = \frac{200\ mA}{4\ V^2} = 50\ mA/V^2$$

Now calculate I_D for $V_{GS} = 3.13$ V.

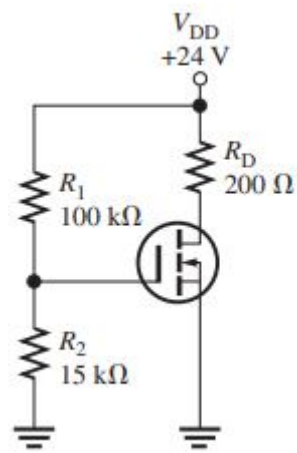
$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\ mA/V^2)(3.13\ V - 2\ V)^2$$
$$= (50\ mA/V^2)(1.13\ V)^2 = 63.8\ mA$$

Finally, calculate V_{DS}.

$$V_{DS} = V_{DD} - I_D R_D = 24\ V - (63.8\ mA)(200\ \Omega) = \mathbf{11.2\ V}$$

H.W: Q10:

Determine VGS and VDS for the circuit in this figure given $I_{D(ON)} = 100\ mA$ at $V_{GS} = 4\ V$ and $V_{GS(th)} = 3\ V$.



Solution:

KEY TERMS:

Depletion In a MOSFET: The process of removing or depleting the channel of charge carriers and thus decreasing the channel conductivity.

Drain: One of the three terminals of a FET analogous to the collector of a BJT.

Enhancement In a MOSFET: The process of creating a channel or increasing the conductivity of the channel by the addition of charge carriers.

Gate: One of the three terminals of a FET analogous to the base of a BJT

JFET: Junction field-effect transistor; one of two major types of field-effect transistors.

MOSFET: Metal oxide semiconductor field-effect transistor; one of two major types of FETs; sometimes called IGFET for insulated-gate FET.

Pinch-off voltage: The value of the drain-to-source voltage of a FET at which the drain current becomes constant when the gate-to-source voltage is zero.

Source: One of the three terminals of a FET analogous to the emitter of a BJT.

Transconductance (g_m): The ratio of a change in drain current to a change in gate-to-source voltage in a FET.

SELF-TEST: https://pinoybix.org/2019/12/self-test-in-field-effect-transistors-floyd.html

1. The JFET is
   (a) a unipolar device (b) a voltage-controlled device
   (c) a current-controlled device (d) answers (a) and (c) (e) answers (a) and (b)
2. The channel of a JFET is between the
   (a) gate and drain (b) drain and source (c) gate and source (d) input and output
3. A JFET always operates with
   (a) the gate-to-source pn junction reverse-biased
   (b) the gate-to-source pn junction forward-biased
   (c) the drain connected to ground
   (d) the gate connected to the source
4. For $V_{GS} = 0\,V$, the drain current becomes constant when V_{DS} exceeds
   (a) cutoff (b) V_{DD} (c) V_P (d) 0 V
5. The constant-current region of a FET lies between
   (a) cutoff and saturation (b) cutoff and pinch-off
   (c) 0 and I_{DSS} (d) pinch-off and breakdown
6. I_{DSS} is
   (a) the drain current with the source shorted (b) the drain current at cutoff
   (c) the maximum possible drain current (d) the midpoint drains current
7. Drain current in the constant-current region increases when
   (a) the gate-to-source bias voltage decreases
   (b) the gate-to-source bias voltage increases
   (c) the drain-to-source voltage increases
   (d) the drain-to-source voltage decreases
8. In a certain FET circuit, $V_{GS} = 0\,V$, $V_{DD} = 15\,V$, $I_{DSS} = 15\,mA$, and $R_D = 470\Omega$. If R_D is decreased to 330Ω, I_{DSS} is
   (a) 19.5 mA (b) 10.5 mA (c) 15 mA (d) 1 mA
9. At cutoff, the JFET channel is
   (a) at its widest point (b) completely closed by the depletion region
   (c) extremely narrow (d) reverse-biased
10. A certain JFET datasheet gives $V_{GS(off)} = -4V$. The pinch-off voltage V_P,
   (a) cannot be determined (b) is $-4V$ (c) depends on V_{GS} (d) is $+4\,V$
11. The JFET in Question 10
   (a) is an n channel (b) is a p channel (c) can be either

12. For a certain JFET, $I_{GSS} = 10\ nA$ at $V_{GS} = 10\ V$. The input resistance is

(a) $100\ M\Omega$ (b) $1\ M\Omega$ (c) $1000\ M\Omega$ (d) $10\ M\Omega$

13. For a certain p-channel JFET, $V_{GS(off)} = 8\ V$. The value of V_{GS} for an approximate midpoint bias is

(a) 4 V (b) 0 V (c) 1.25 V (d) 2.34 V

14. In a self-biased JFET, the gate is at

(a) a positive voltage (b) 0 V (c) a negative voltage (d) ground

15. A MOSFET differs from a JFET mainly because

(a) of the power rating (b) the MOSFET has two gates

(c) the JFET has a pn junction (d) MOSFETs do not have a physical channel

16. A D-MOSFET operates in

(a) the depletion mode only (b) the enhancement mode only

(c) the ohmic region only (d) both the depletion and enhancement modes

17. An n-channel D-MOSFET with a positive V_{GS} is operating in

(a) the depletion mode (b) the enhancement mode (c) cutoff (d) saturation

18. A certain p-channel E-MOSFET has a $V_{GS(th)} = -2V$. If $V_{GS} = 0\ V$, the drain current is

(a) 0 A (b) $I_{D(ON)}$ (c) maximum (d) I_{DSS}

19. In an E-MOSFET, there is no drain current until V_{GS}

(a) reaches $V_{GS(th)}$ (b) is positive (c) is negative (d) equals 0 V

20. All MOS devices are subject to damage from

(a) excessive heat (b) electrostatic discharge (c) excessive voltage (d) all of these

21. A certain D-MOSFET is biased at $V_{GS} = 0\ V$. Its datasheet specifies $I_{DSS} = 20\ mA$ and $V_{GS(off)} = -5V$. The value of the drain current

(a) is 0 A (b) cannot be determined (c) is 20 mA