Contents

EXPERIMENT NO. (1)

COMMON BASE INPUT AND OUTPUT CHARACTERISTICS

OBJECTIVE:

- To explain saturation and cutoff regions in relation to the curves.
- To understand common base input and output characteristics of BJT transistors.
- To determine the input and output resistance of BJT transistors in common base.

THEORY:

The input characteristic is the relation between I_E and V_{BE} at a constant V_{CB}. This relation is shown in figure 1.1

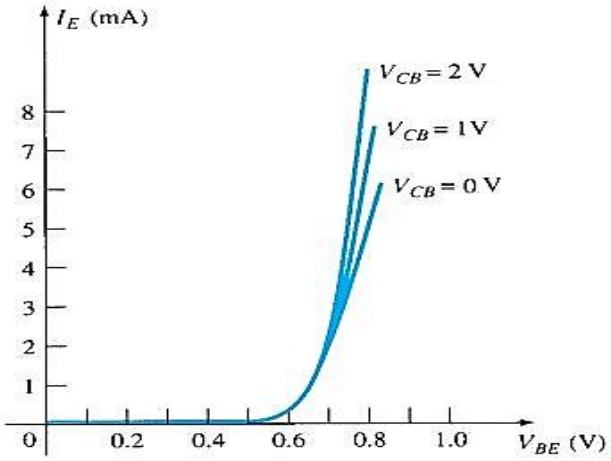


Figure 1.1 Common Base Input Characteristic

While the output characteristic is the relation between Ic and V_{CB} at a constant I_E. This relation is shown in figure 1.2

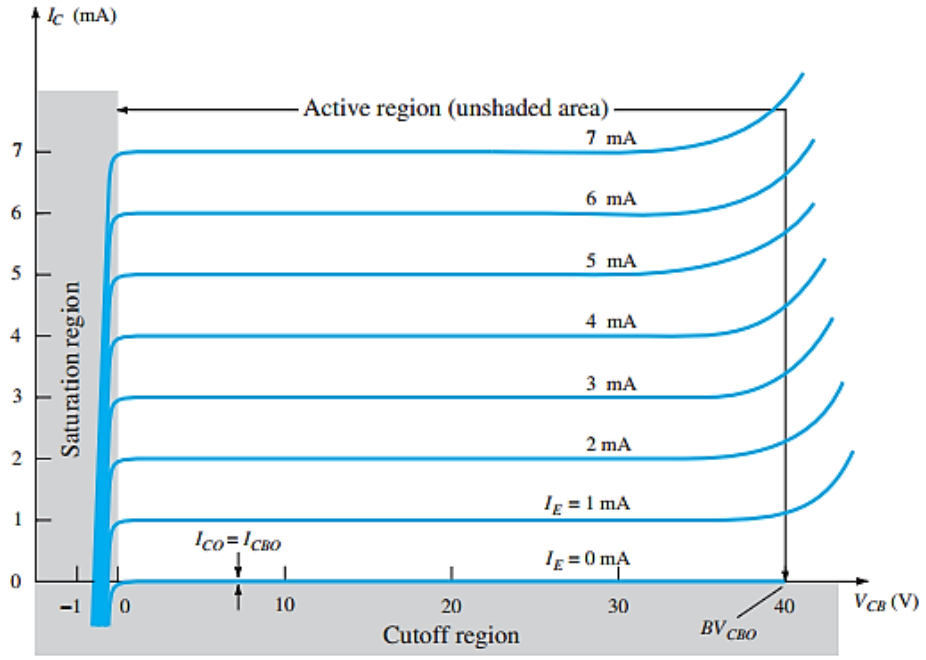


Figure 1.2 Common Base Output Characteristic

REQUIRED ELEMENTS:

Element	Quantity	Value/Type
Resistor	2	1 k Ohm
Transistor	1	C945
DC Voltage Source	2	
Multi-meters	3	
Wires		

CIRCUITS:

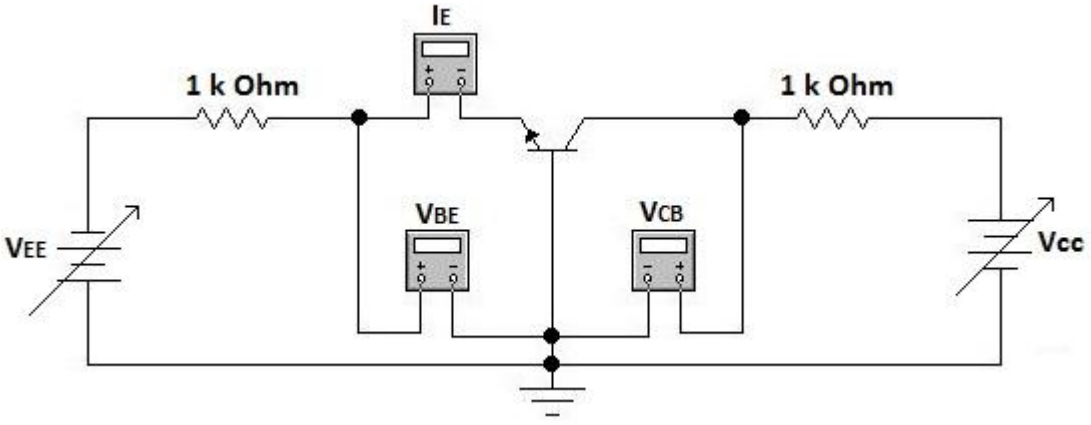


Figure 1.3

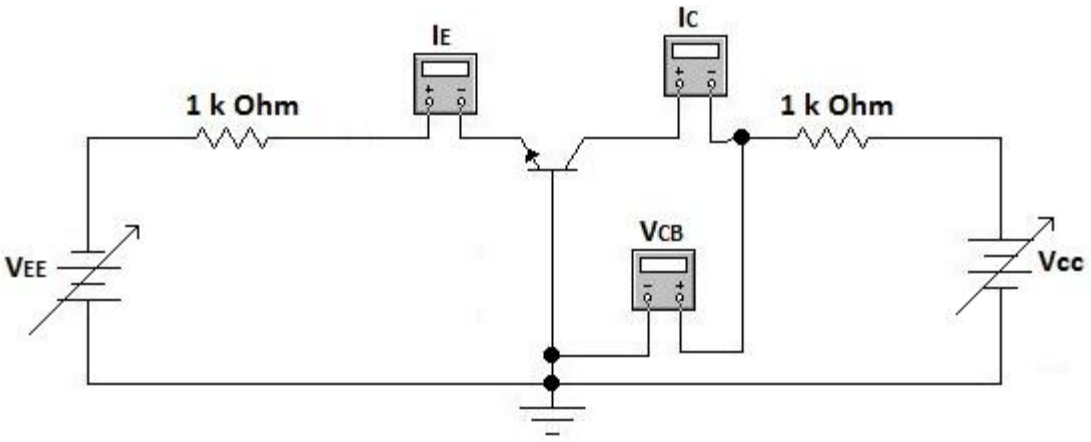


Figure 1.4

PROCEDURE:

1- Input characteristic

a- Connect the circuit shown in figure 1.3
b- Change V_{CC} to make $V_{CB} = 0$.
c- Change V_{BE} by using V_{EE} from 0 to 0.9V steps 0.1V, and record I_E at each step.
d- Repeat step **c** for $V_{CB} = 2V$.

V_{BE} (V)	I_E when $V_{CB} = 0V$	I_E when $V_{CB} = 2V$
0		
0.1		
0.2		
0.3		
0.4		
0.5		
0.6		
0.7		
0.8		
0.9		

Table 1.1 Results for input characteristic

2- Output characteristic

a- Connect the circuit shown in figure 1.4
b- Adjust I_E at 0 by using V_{EE}.
c- Change V_{CB} from 0 to 10V step 1, and record I_C for each step.
d- Repeat step **c** for $I_E = 1mA$, and 2mA

V_{CB} (V)	I_C when $I_E = 0$ mA	I_C when $I_E = 1$ mA	I_C when $I_E = 2$ mA
0			
1			
2			
3			
4			

5			
6			
7			
8			
9			
10			

Table 1.2 Results for output characteristic

CALCULATION, QUESTION AND DISCUSSION

1- From the obtained results, draw the input and output characteristics.
2- From the input characteristic, find the input resistance.
3- From the output characteristic, find the output resistance and the current gain.
4- What are the advantages of this type of connection?
5- Define the reverse saturation current I_{CO}.
6- Discuss your experimental results.

EXPERIMENT NO. (2)

COMMON EMITTER INPUT AND OUTPUT CHARACTERISTICS

OBJECTIVE:

- To understand common emitter input and output characteristics of BJT transistors.
- To determine the input and output resistance of BJT transistors in common emitter.

THOERY:

The most frequently encountered transistor configuration for the BJT transistors is called the common-emitter configuration because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals). The input curve is the relation between I_B and V_{BE} at constant V_{CE} as shown in figure 2.1.

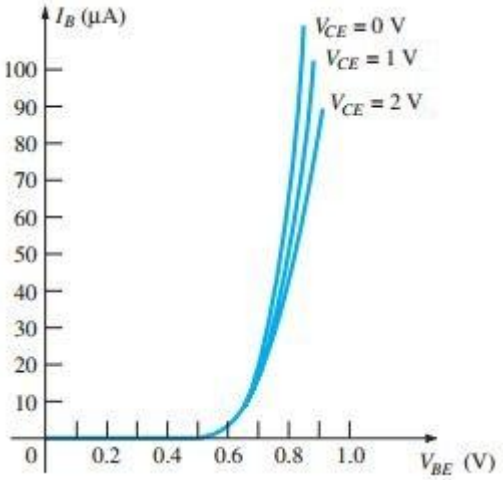


Figure 2.1 Common emitter input characteristic

While the output curve is the relation between I_C and V_{CE} at constant value of I_B. The output characteristic is shown in figure 2.2.

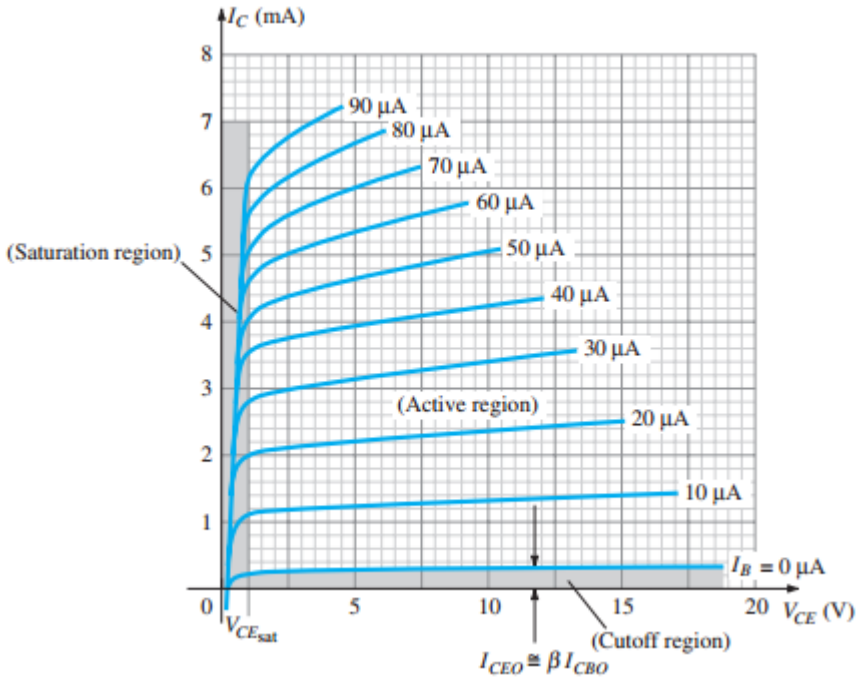


Figure 2.2 Common emitter output characteristic

REQUIRED ELEMENTS:

Element	Quantity	Value/Type
Resistor	2	1 k Ohm
Transistor	1	C945
DC Voltage Source	2	
Multi-meters	3	
Wires		

CIRCUITS:

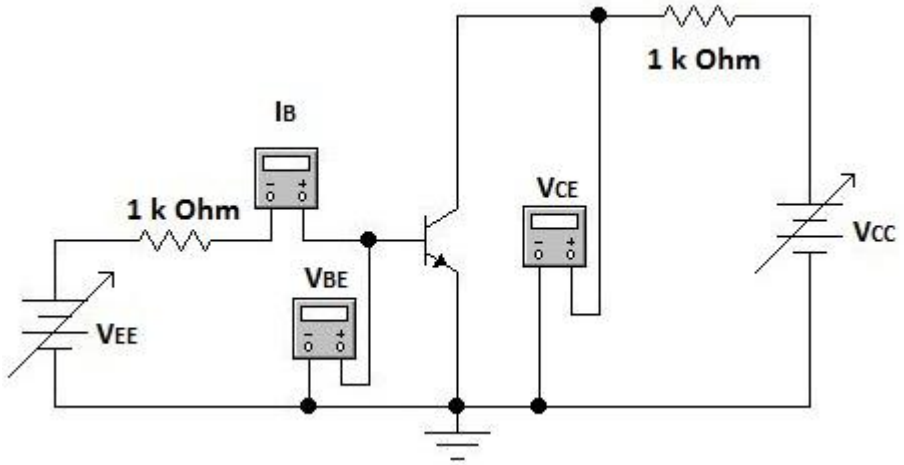


Figure 2.3

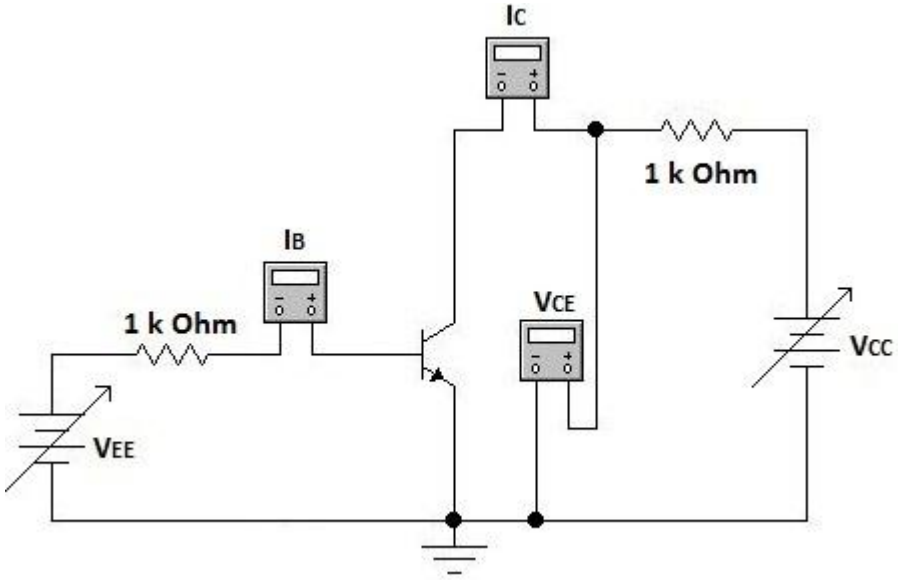


Figure 2.4

PROCEDURE:

1- Input characteristic

a- Connect the circuit shown in figure 2.3

b- Change V_{CC} to make $V_{CE} = 0$.

c- Change V_{BE} by using V_{EE} from 0 to 0.9V steps 0.1V, and record I_B at each step.

d- Repeat step **c** for $V_{CE} = 2V$.

V_{BE} (V)	I_B when $V_{CE} = 0V$	I_B when $V_{CE} = 2V$
0		
0.1		
0.2		
0.3		
0.4		
0.5		
0.6		
0.7		

0.8		
0.9		

Table 2.1 Results for input characteristic

2- Output characteristic

a- Connect the circuit shown in figure 2.4
b- Adjust I_B at 0 by using V_{EE}.
c- Change V_{CE} from 0 to 7V step 1, and record I_C for each step.
d- Repeat step **c** for I_B = 20μA, and 40μA

V_{CE} (V)	I_C when I_B = 0 A	I_C when I_B = 20μA	I_C when I_B = 40μA
0			
1			
2			
3			
4			
5			
6			
7			

Table 2.2 Results for output characteristic

CALCULATION, QUESTION AND QUESTION:

1- Draw the input characteristic from the result of part 1 of the experiment.
2- Find the input resistance from the input curve.
3- Draw the output characteristic from the results of part 2 of the experiment.
4- Find the output resistance and the current gain from the output curve.
5- What are the advantages of this kind of configuration?
6- Discuss your experimental result.

EXPERIMENT NO. (3)

TRANSISTOR BASING CIRCUITS – FIXED BIAS

OBJECTIVE:

- To describe and draw a dc load line.
- To define the Q point.
- To know the effect of temperature on Q point.

THEORY:

A transistor must be properly biased with a dc voltage in order to operate as a linear amplifier. A dc operating point (Q point) must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. The best case is to set Q point at the center. The fixed bias circuit is one of the circuit which makes the transistor operates in the active region. In this circuit, I_C can be adjusted at the center by varying R_B or R_C or R_E in order to make Q point at the center of load line.

REQUIRED ELEMENTS:

Element	Quantity	Value/Type
Resistor	2	1 k Ohm, 820 Ohm
Transistor	1	C945
DC Voltage Source	1	
Multi-meters	2	
Wires		

PROCEDURE:

1- Connect the circuit shown in figure 3.1
2- For R_B = 220 kΩ and R_E = 0 Ω (short circuit), measure the ammeter I_C and voltmeter V_{CE} readings.
3- Repeat step 2 when R_B = 470 kΩ.

When R_E = 0		
R_B	I_C	V_{CE}
220 kΩ		
470 kΩ		

Table 3.1 Table for results from step 2 and 3

4- Repeat step 2 and 3 when R_E exists and equal 820 Ω.

When R_E = 820 Ω		
R_B	I_C	V_{CE}
220 kΩ		
470 kΩ		

Table 3.1 Table for results from step 4

5- Increase the transistor temperature and observe ammeter I_C and voltmeter V_C readings, where
A) R_B = 220 kΩ and R_E = 0 Ω
B) R_B = 220 kΩ and R_E = 820 Ω

CIRCUIT:

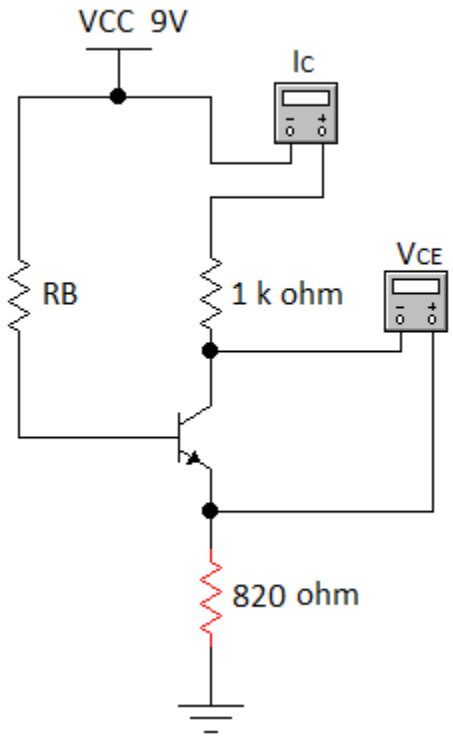


Figure 3.1

CALCULATIONS, QUESTIONS AND DISCUSSION:

1- Draw the DC load line and denote Q point from your practical results for all cases.
2- Draw the DC load line and denote Q point theoretically for all cases. Assume that βdc = 200.
3- What is the effect of temperature on the operating point?
4- What is the effect of R_E and R_B on the operating point?
5- Discuss your results.

EXPERIMENT NO. (4)

TRANSISTOR BASING CIRCUITS – VOLTAGE DIVIDER

OBJECTIVE:

- To know the effect of resistor values on the basing

- To describe the dc load line and Q-point.

THEORY:

The voltage divider bias is the most widely used circuit arrangement in transistor applications especially amplifiers. A base voltage is developed by resistive voltage divider. The voltage divider bias has more advantages than fixed bias. The effect of temperature is less and designers have more chance to design the desire circuit. Therefore, this circuit has more applications than any other biasing circuits.

PROCEDURE:

1- Connect the circuit shown in figure (4.1)
2- For R_2 = 470 Ω, R_C = 1 KΩ, R_E = 1 KΩ, change R_1 from 0 to a suitable value and record I_C and V_{CE} in table 4.1. **Note:** Please do not let I_C exceed 1.5 mA.
3- For R_1 = 33 KΩ, R_C = 1 KΩ, R_E = 1 KΩ, change R_2 from 0 to a suitable value and record I_C and V_{CE} in table 4.2

R1 Ω	I_C	V_{CE}
0		
100		
200		
300		
400		
500		
600		
700		
800		
900		
1k		
2k		

Table 4.1

R2 kΩ	I_C	V_{CE}
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
12		

Table 4.2

4- For R_1 = 33 KΩ, R_2 = 4.7KΩ, R_E = 1 KΩ, change R_C to set the Q-point at the center of the dc-load line, and then record I_C and V_{CE}.

CIRUIUT:

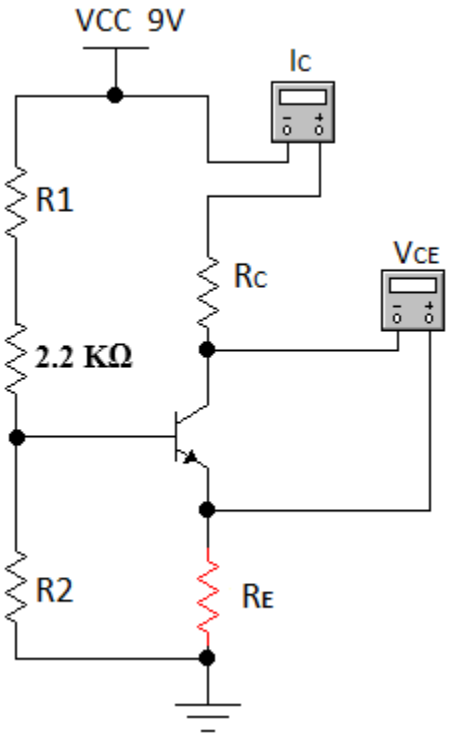


Figure 4.1 Voltage Divider bias

CALCULATIONS, QUESTIONS AND DISCUSSION:

1- Draw the relation between (R1 vs I_C), and (R1 vs V_{CE}) separately.
2- Draw the relation between (R2 vs I_C), and (R2 vs V_{CE}) separately.
3- Draw the dc-load line for the value of R_C which has practically been found to set the Q-point at the center.
4- Why 2.2 KΩ is connected in series with R1?
5- Discuss your practical result.

EXPERIMENT NO. (5)

COMMON EMITTER AMPLIFER CHARACTERSTICS

OBJECTIVE:

- Identify ac quantities
  - Distinguish ac quantities from dc quantities
- Describe the voltage gain
- To find the input resistance
- Define phase inversion

THEORY:

In a common emitter amplifier, the input signal is applied to base-emitter side, and the output is taken from the collector-emitter side of the transistor. To analyze the amplifier shown in figure (5.1), the dc bias values (voltages and currents) must be determined while the capacitors are replaced with open cct.

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

$$V_E = V_B - 0.7$$

$$We\ know\ that\ \ I_E = \frac{V_E}{R_E}$$

$$V_{CC} = V_C - I_C R_C$$

$$I_C \cong I_E$$

For ac analyzing, the capacitors and the DC source are replaced with short cct (Xc = 0).

The ac resistance of emitter is

$$r_e = \frac{25mv}{I_E}$$

And the voltage gain is:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_c\ (R_c \,||\, R_L)}{I_c\ r_e} = \frac{(R_c \,||\, R_L)}{r_e}$$

$$Therefore \quad Vc = A_v\ Vb$$

And the total input resistance is $R1 \,||\, R2 \,||\, \beta_{dc}\ r_e$

PROCEDURE:

1- Theoretically compute the dc parameters listed in the table (5.1) using above equations and records them in the table.
2- Practically measure and record the dc parameters listed in table (5.1).
3- Compute the ac parameters listed in table (5.2).
4- Turn on the signal generator and set V_s to 10 mVp-p and 1 kHz. Use the ac source as the input voltage (V_{be}) to the circuit, and measure the ac output voltage and the voltage gain.
5- To find the R_{in}, a variable test resistance (R_{test}) is connected in series with C1. Increase R_{test} until V_{out} drops to half of the previous value. This means that half of the input ac voltage (V_s) is dropped on the R_{test} and the other half on Rin.

   $R_{in} = R_{test}$
6- Use both channels of the oscilloscope to compare the input and output waveforms. What is the phase relationship between V_{in} and V_{out}?
7- Remove C_E from the circuit, and measure the voltage gain. What can be concluded from this action?
8- Replace C_E and remove R_L, after that measure Av.

DC parameters	Computed values	Measured values
V_B		
V_E		
I_E		
V_C		
V_{CE}		

Table 5.1

DC parameters	Computed values	Measured values
V_b		
V_e		
r_e		
A_V		
V_C		
Rin		

CIRCUIT:

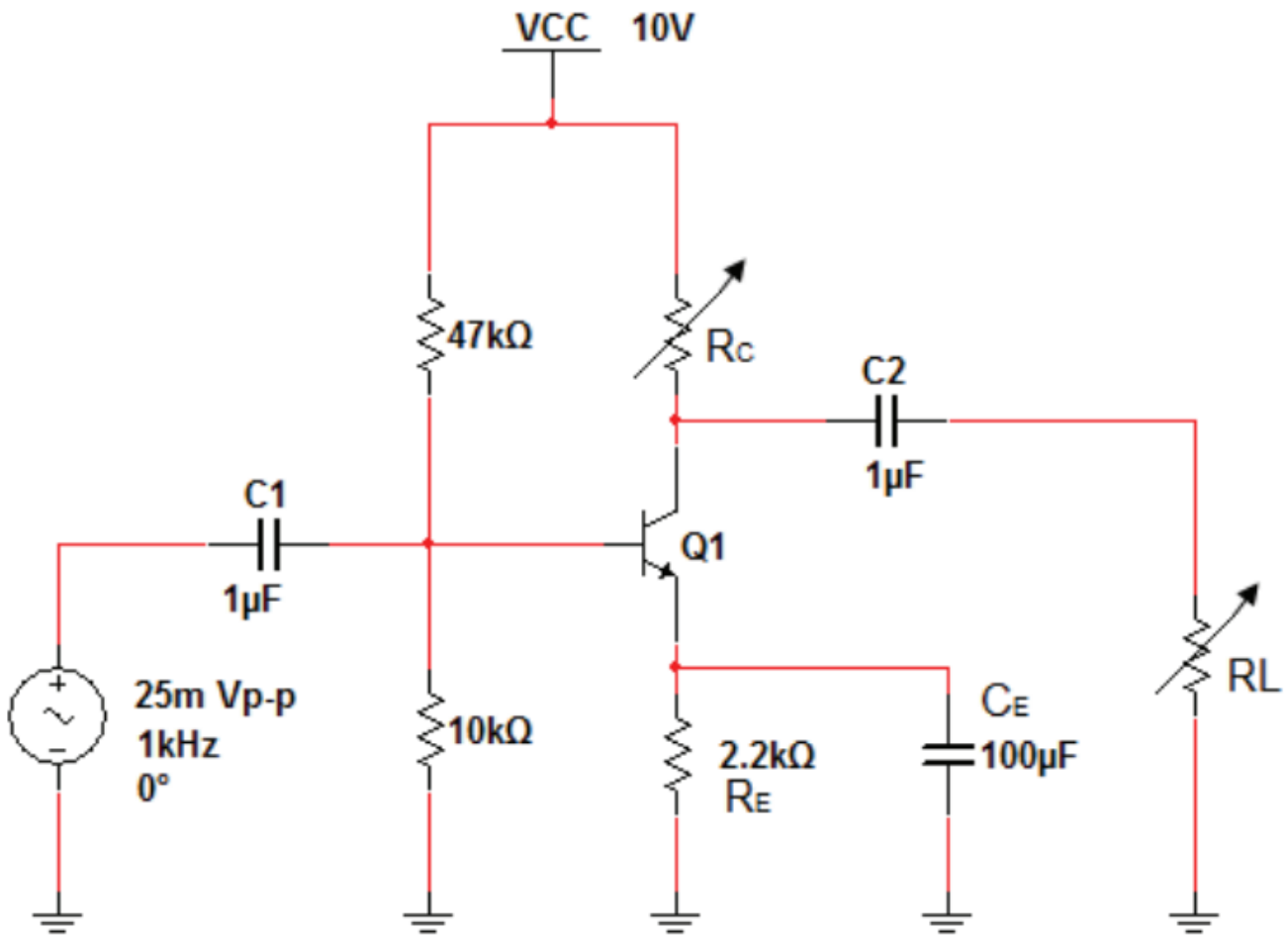


Figure 5.1 the amplifier circuit

CALCULATION, QUESTION AND DISCUSSION

1- When C_E is open, you found that the gain was affected. Explain it why?
2- Discuss your results

EXPERIMENT NO. (6)

COMMON COLLECTOR AMPLIFER CHARACTERSTICS

OBJECTIVE:

- Discuss the emitter-follower amplifier with voltage-divider bias
- Current gain vs. Voltage gain in common-collector amplifier

THEORY:

When the output is taken from the emitter terminal of the transistor as shown in Figure 6.1 , the network is referred to as an *emitter-follower*. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $Av \cong 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal *Vi*. That is, both *Vo* and *Vi* attain their positive and negative peak values at the same time. The fact that *Vo* "follows" the magnitude of *Vi* with an in phase relationship accounts for the terminology emitter-follower.

This configuration has high input impedance, a low output impedance and high current gain.

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

$$V_E = V_B - 0.7$$

$$We\ know\ that\ I_E = \frac{V_E}{R_E}$$

$$V_{CC} = V_C$$

$$I_C \cong I_E$$

$$V_{CE} = V_{CC} - V_E$$

For ac analyzing, the capacitors and the DC source are replaced with short cct (Xc = 0).

The ac resistance of emitter is

$$r_e = \frac{25mv}{I_E}$$

$V_{out} = I_e R_e$ Where $R_e = R_E || R_L$

$$V_{in} = I_e(r_e + R_e)$$

Therefore the voltage gain is

$$Av = \frac{I_e R_e}{I_e(r_e + R_e)} = \frac{R_e}{(r_e + R_e)}$$ If $R_e >> r_e$ then $Av \cong 1$

$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b} = \frac{I_e(r_e + R_e)}{I_b}$$

$$Since\ I_e \cong\ I_c = \beta\ I_b$$

$$R_{in(base)} = \frac{\beta\ I_b(r_e + R_e)}{I_b}$$

The terms I_b cancel; therefore,

$$R_{in(base)} = \beta(r_e + R_e)$$

$$R_{in(total)} = R_1 \,||\, R_2 \,||\, R_{in(base)}$$

$$A_P = \frac{\left(\frac{V_O}{R_{O(total)}}\right)^2}{\left(\frac{V_i}{R_{in(total)}}\right)^2} = {A_V}^2 \left(\frac{R_{in(total)}}{R_{O(total)}}\right)^2 \cong \left(\frac{R_{in(total)}}{R_{O(total)}}\right)^2$$

$$R_{O(total)} = (\frac{R_1 \,||\, R_2 \,||\, R_S}{\beta}) \,||\, (R_E + r_e)$$

$$R_{O(total)} \cong (\frac{R_S}{\beta}) \,||\, (R_E + r_e) \qquad When\ \ (R_1 \,||\, R_2) \gg R_S$$

PROCEDURE:

1- Theoretically compute the dc parameters shown in table 6.1
2- Practically measure the dc parameters shown in table 6.1
3- Theoretically compute the ac parameters shown in table 6.2
4- Practically measure the ac parameters shown in table 6.2 for Vs = 1 Vp-p and 1 kHz.
5- Measure the input resistance using the same method that you used in the last experiment.
6- Use two channels of the oscilloscope figure out the phase difference between Vin and Vo.

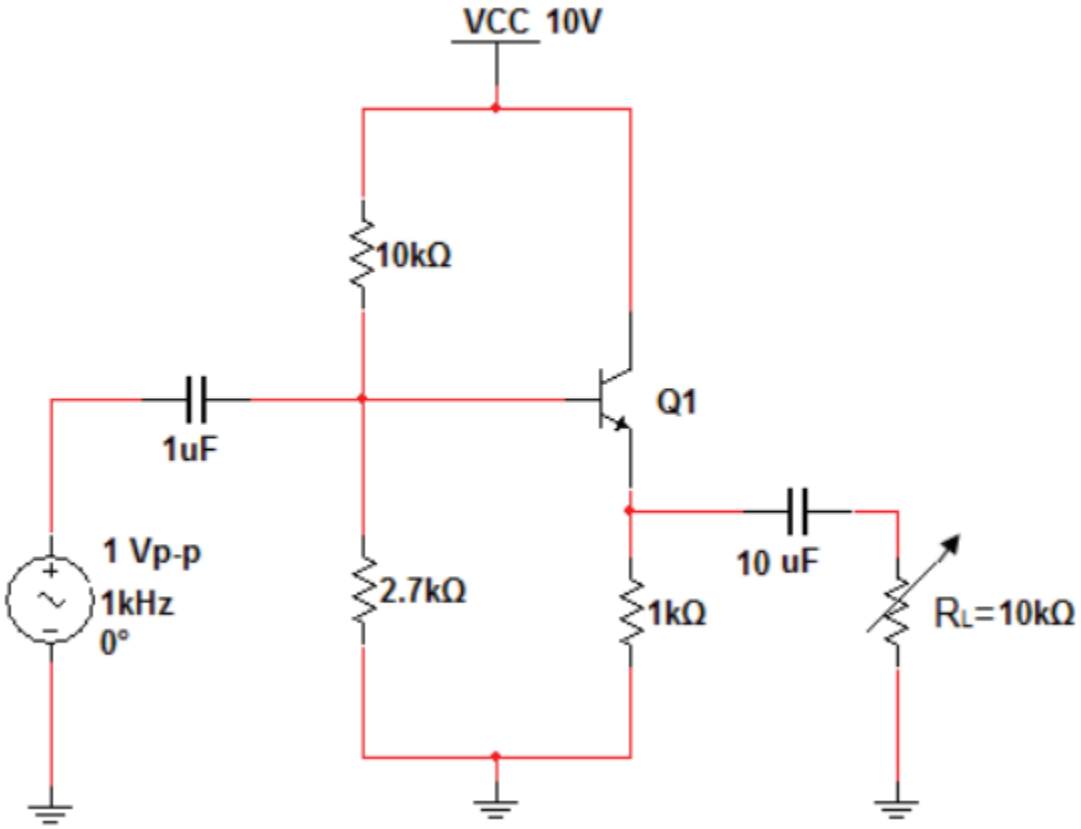
DC parameters	Computed values	Measured values
V_B		
V_E		
I_E		
V_C		
V_{CE}		

Table 6.1 DC parameters

AC parameters	Computed values	Measured values
V_b		
V_e		
r_e		
A_V		
R_{in}		
A_p		

Table 6.1 AC parameters

CIRCUIT:



CALCULATION, QUESTION AND DISCUSSION

1- Compare the input resistance of C.E.A and C.C.A.
2- Compare the phase difference of C.E.A and C.C.A.
3- The emitter follower can be used to drive a low impedance load such as loudspeakers. What characteristic makes this circuit for this purpose?
4- Discuss your results.

EXPERIMENT NO. (7)

FILED EFFECT TRANSISTOR OUTPUT CHARACTERSISTICS

OBJECTIVE:

- To discuss the drain characteristic curve
- To identify the ohmic, active, and breakdown regions of the curve
- To explain how gate-to-source voltage controls the drain current

THEORY:

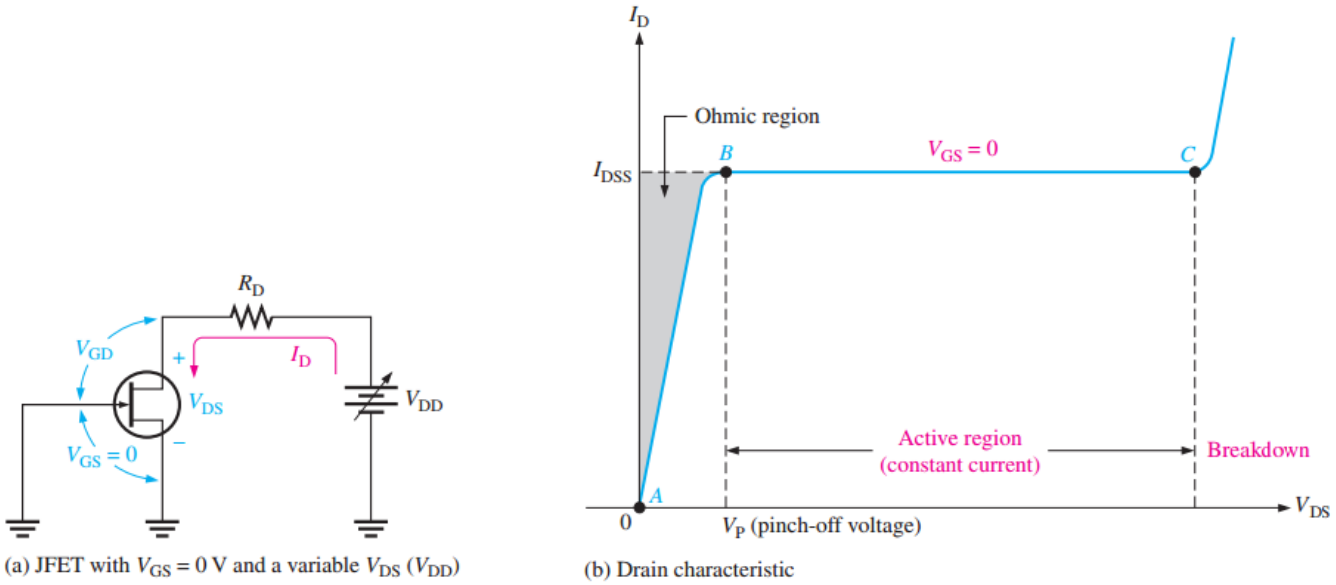
The term field-effect relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminals (gate). Recall that a BJT is a current-controlled device; that is, the base current controls the amount of collector current. A FET is different. It is a voltage-controlled device, where the voltage between two of the terminals (gate and source) controls the current through the device.

Drain Characteristic Curve

Consider the case when the gate-to-source voltage is zero (V_{GS} = 0 V). This is produced by shorting the gate to the source, as in Figure 7–1(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Figure 7–1(b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ***ohmic region*** because V_{DS} and I_D are related by Ohm's law.

At point B in Figure 7–1(b), the curve levels off and enters the active region where I_D becomes essentially constant. As V_{DS} increases from point B to point C, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

The value of V_{DS} at which I_D becomes essentially constant (point B on the curve in Figure 7–1(b)) is the pinch-off voltage, V_P. For a given JFET, V_P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (Drain to Source current with gate Shorted) and is always specified on JFET datasheets. I_{DSS} is the maximum drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, V_{GS} = 0 V.



(a) JFET with V_{GS} = 0 V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

The drain characteristic curve of a JFET for V_{GS} = 0 showing pinch-off voltage.

As V_{GS} is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure 7–2(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel.

The value of V_{GS} that makes I_D approximately zero is the **cutoff voltage,** $V_{GS(off)}$, as shown in Figure 7–2(d). The JFET must be operated between $V_{GS} = 0$ V and $V_{GS(off)}$.

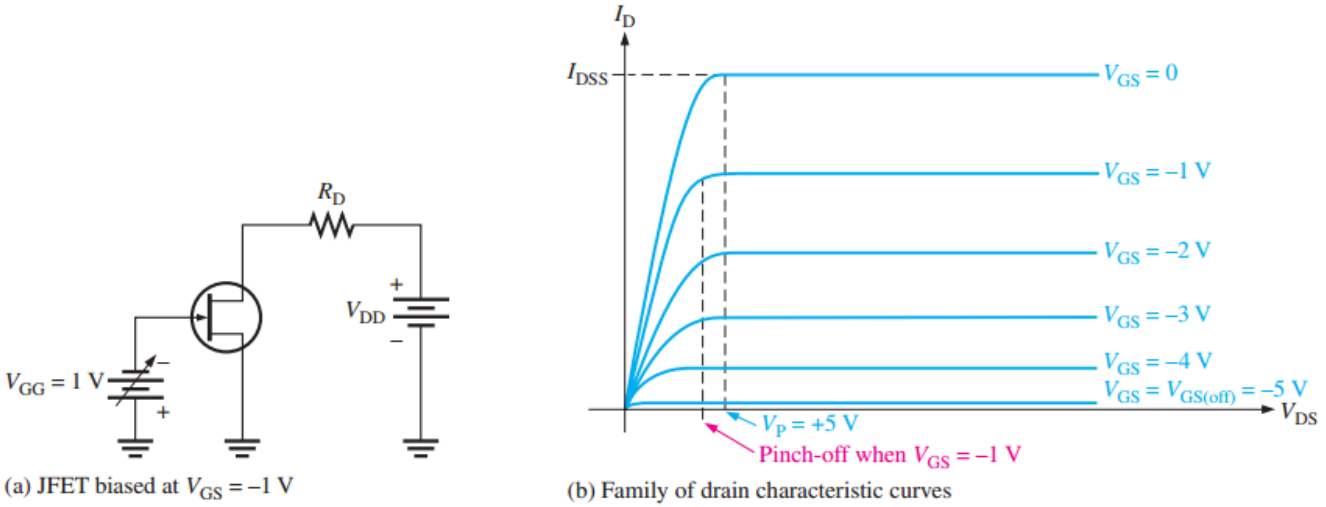


Figure 7.2 Family of Drain Characteristic

PROCEDURE:

1- Connect the circuit shown in figure (7.3)
2- By using V_{GG} source, adjust $V_{GS} = 0$V.
3- Change V_{DS} from 0 to 8V using the V_{DD} source and measure I_D, and fill table 7.1.
4- Repeat step 2 and 3 for VGS = 1V, and 2V.

V_{DS} (volt)	I_D when $V_{GS} = 0$ V	I_D when $V_{GS} = 1$ V	I_D when $V_{GS} = 2$ V
0			
1			
2			
3			
4			
5			
6			
7			
8			

Table 7.1

CIRCUIT:

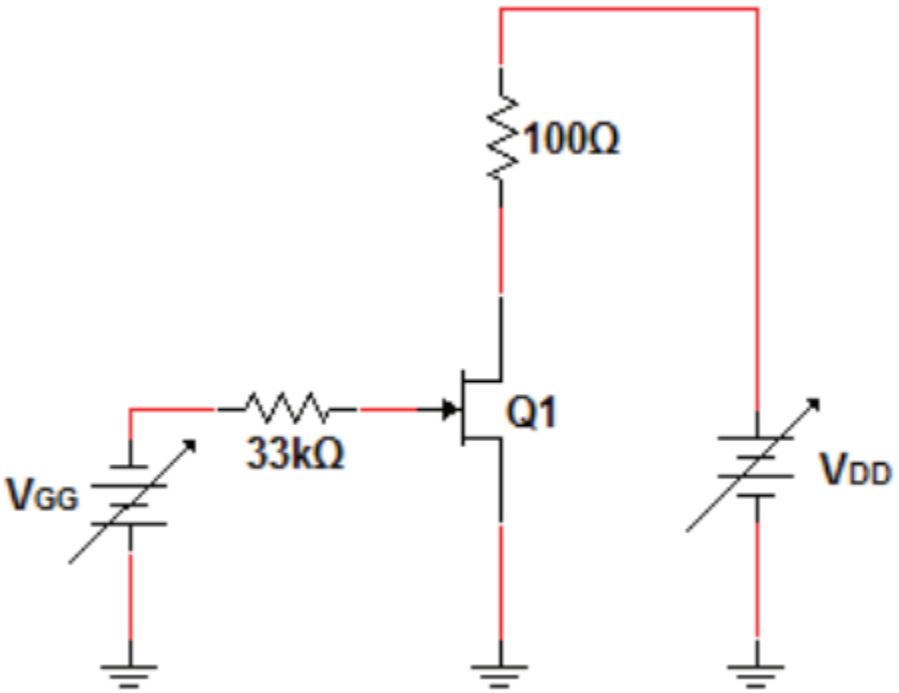


Figure 7.3

CALCULATION, QUESTION AND DISSCUSSION:

1- Use your practical results to draw the drain characteristic curve.
2- Find I_{DSS} from the characteristic curve.
3- Compare the pinch off voltage, V_P, with cut off, $V_{GS\ (off)}$.
4- Discuss your results.

EXPERIMENT NO. (8)

COMMON SOURCE FILED EFFECT TRANSISTOR AMPLIFER

OBJECTIVE:

- To explain and analyze the operation of common-source FET amplifiers.
- To discuss and analyze the FET ac model.
- To observe phase inversion.

THEORY:

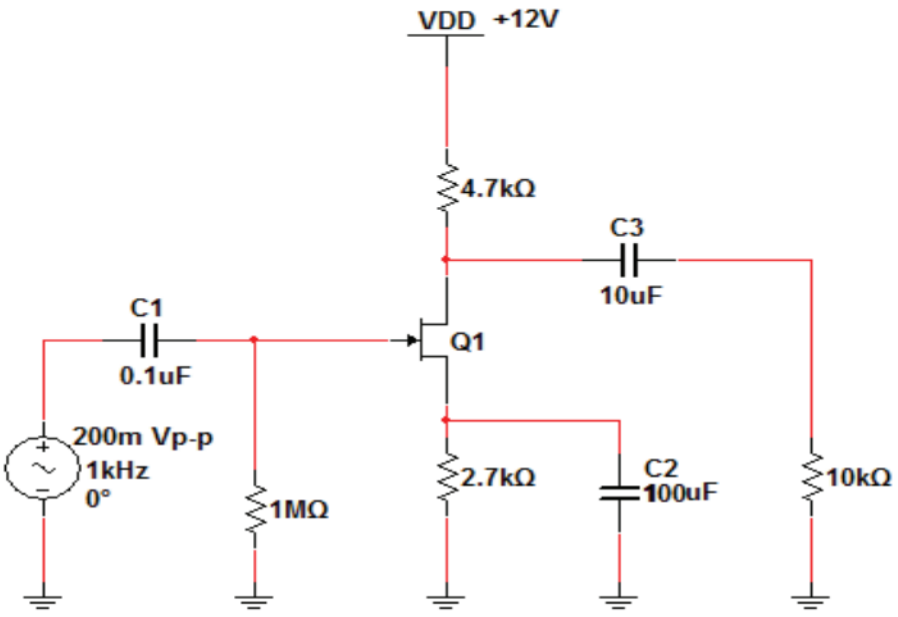
The FET has an important advantage compared to the BJT due to the FET's extremely high input impedance. Disadvantages, however, include higher distortion and lower gain. The particular application will usually determine which type of transistor is best suited. The common-source (CS) amplifier is comparable to the common-emitter BJT amplifier.

Note: For more details about DC and AC analysis, please review your theoretical lectures.

PROCEDURE:

1- Connect the circuit shown in figure 8.1.
2- Set the signal generator at 200m Vp-p and 1 kHz.
3- Measure the DC voltages at drain (V_D), source (V_S), gate (V_G), and V_{DS}. Then measure I_D
4- Measure the input and output AC voltages, and then find the voltage gain.
5- Remove the bypass capacitor and then measure the gain (measure input and output voltages).
6- Compare the phase difference between input and output voltages.

CIRCUIT:



CALCULATION, QUESTION AND DISSCUSSION:

1- Compare the voltage gain of common source FET amplifier with its analogy common emitter BJT amplifier. Which one has higher voltage gain? Use your results to make this comparison.
2- Discuss you results.

EXPERIMENT NO. (9)
THE JFET AS AN ANALOG SWITCH

OBJECTIVE:

- To explain how FETs can be used in analog switching applications
- To Explain how a FET operates as a switch

THEORY:

An analog switch is an electronically controlled device that will either pass or shut off continuously varying analog signal. Figure 9.1 illustrates an analog switch. In most cases, a digital signal is used to control switching process.

A JFET can be used an analog switch as shown in figure 9.2. Note that the analog signal is connected to R_D where a fixed supply voltage (V_{DD}) would normally be connected. The digital signal that opens and closes the switch is the gate to source voltage V_{GS}. V_{GS} is either (0V) which makes the JFET on (conducting) or V_P (a negative voltage for N-channel) that makes the JFET off. The output voltage of the switch V_O is the drain to source voltage which will be either the analog signal (when the JFET is off) or zero (when the JFET is conducting)

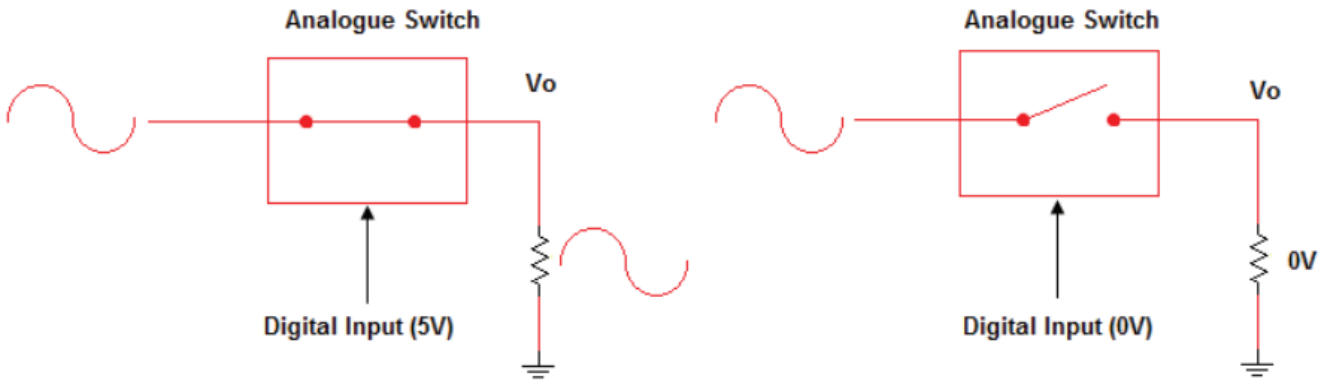


Figure 9.1 a normal switch operation

CIRCUIT:

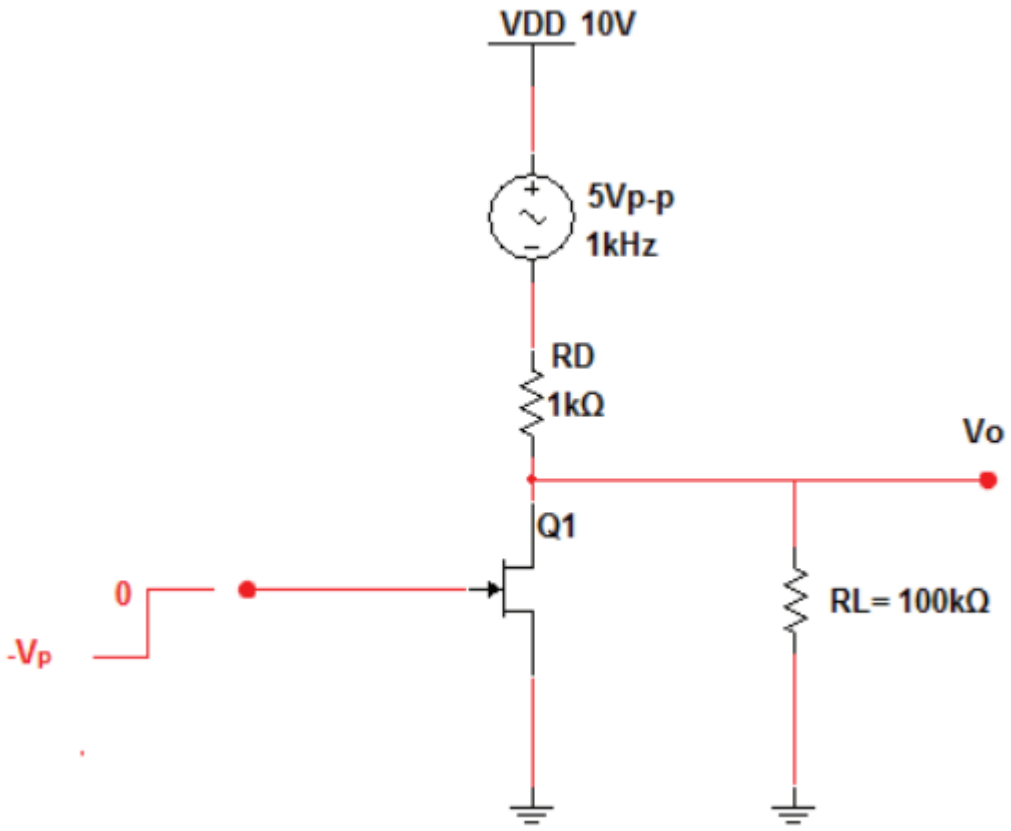


Figure 9.2 JFET as a switch

PROCEDURE:

1- Practically measure V_P for the JFET. Use the same method of previous experiment.
2- Connect the circuit as shown in figure 9.2.
3- Make $V_{GS} = 0$, and then observe the output and draw the output signal.
4- Make $V_{GS} = V_P$, and then observe the output and draw the output signal.

CALCULATION, QUESTIONS AND DISCUSSION:

1- What is R_{DSon}?
2- Can we use BJT as a switch? If yes, which type of transistor (FET or BJT) performs better as a switch? And why?
3- Discuss your results.

EXPERIMENT NO. (10)
FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFER

OBJECTIVE:

- To explain how circuit capacitances affect the frequency response of an amplifier.
- To analyze the low-frequency response of an amplifier.
- To analyze the high-frequency response of an amplifier.
- To analyze an amplifier for total frequency response
- To measure the frequency response of an amplifier

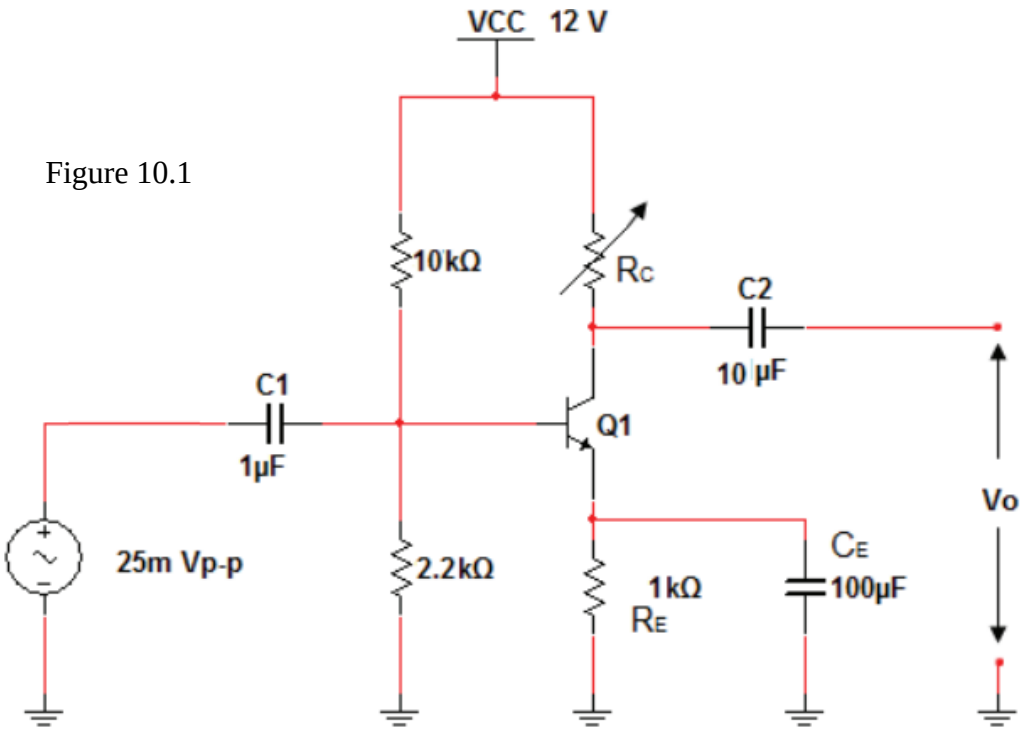
THEORY:

In the previous chapters on amplifiers, the effects of the input frequency on an amplifier's operation due to capacitive elements in the circuit were neglected in order to focus on other concepts. The coupling and bypass capacitors were considered to be ideal shorts and the internal transistor capacitances were considered to be ideal opens. This treatment is valid when the frequency is in an amplifier's midrange. As you know, capacitive reactance decreases with increasing frequency and vice versa. When the frequency is low enough, the coupling and bypass capacitors can no longer be considered as shorts because their reactances are large enough to have a significant effect. Also, when the frequency is high enough, the internal transistor capacitances can no longer be considered as opens because their reactances become small enough to have a significant effect on the amplifier operation. A complete picture of an amplifier's response must take into account the full range of frequencies over which the amplifier can operate.

Recall from basic circuit theory that $Xc = {}^{1}/_{2\pi fC}$ This formula shows that the capacitive reactance varies inversely with frequency. At lower frequencies the reactance is greater, and it decreases as the frequency increases.

CIRCUIT:

Figure 10.1



PROCEDURE:

1- Connect the circuit shown in figure 10.1
2- Change R_C to obtain the Q point at the center of DC load line.
3- Change the input frequency from 10 Hz to 5 MHz, and measure V_O for each frequency.

Input Frequency (Hz)	Output Voltage (V)
10	
20	
30	
:	
:	
100	
200	
300	
:	
:	
1 k	
2 k	
3 k	
:	
:	
10 k	
20 k	
30 k	
:	
:	
100 k	
200 k	
300 k	
:	
:	
1 M	
2 M	
3 M	

CALCULATION, QUESTIONS AND DISCUSSION:

1- From your practical results, plot Vo vs the frequency on a semiology paper.
2- From the plot, determine the upper and lower cutoff frequencies.
3- Find the bandwidth.
4- Determine the gain at one octave below the upper cutoff frequency.
5- Determine the gain at one octave above lower cutoff frequency.
6- Discuss your practical results.

EXPERIMENT NO. (11)
FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFER

OBJECTIVE:

- To explain how circuit capacitances affect the frequency response of an amplifier.
- To analyze the low-frequency response of an amplifier.
- To analyze the high-frequency response of an amplifier.
- To analyze an amplifier for total frequency response
- To measure the frequency response of an amplifier

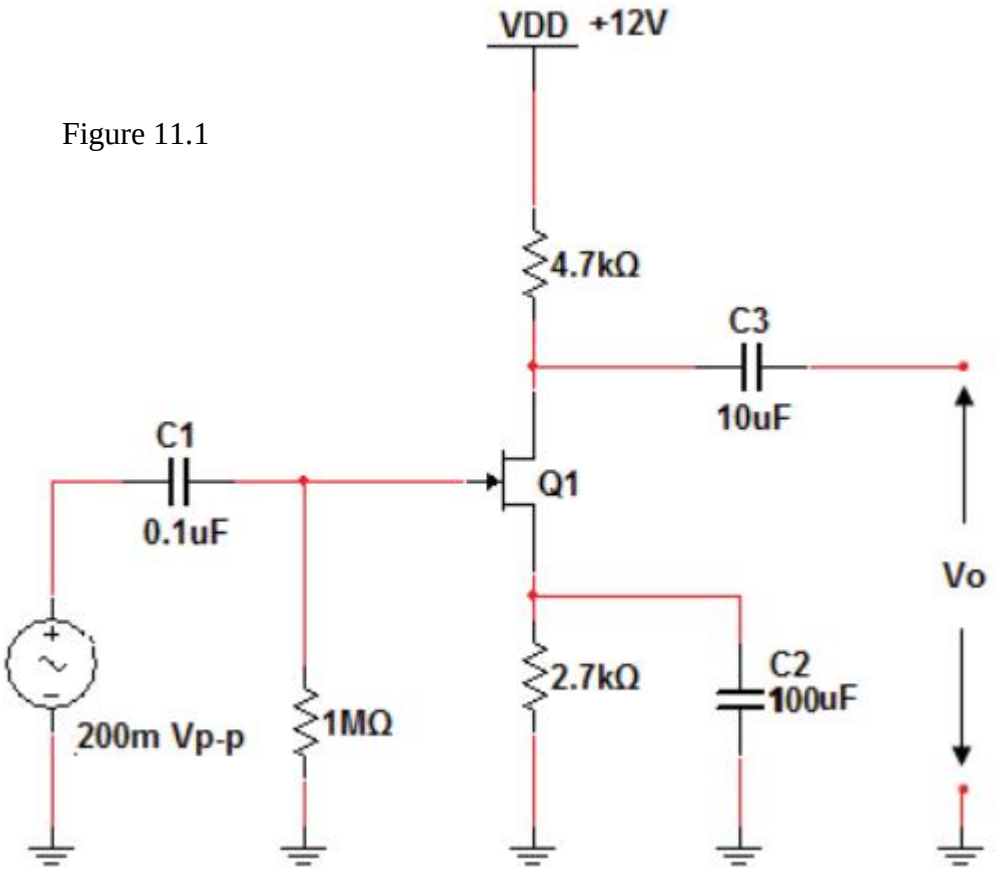
THEORY:

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier. There are again three capacitors of primary concern as appearing in the network of figure 11.1: C1, C2, and C3. As in the case for the BJT amplifier, the reactance (Xc) of the input, output, and bypass coupling capacitors decrease as the input frequency increases.

The approach to the high-frequency analysis of a FET amplifier is also similar to that of a BJT amplifier. The basic differences are the specifications of the internal FET capacitances and the determination of the input resistance.

CIRCUIT:

Figure 11.1



PROCEDURE:

1- Connect the circuit shown in figure 11.1
2- Change the input frequency from 10 Hz to 5 MHz, and measure V_O for each frequency.

Input Frequency (Hz)	Output Voltage (V)
10	
20	
30	
:	
:	
100	
200	
300	
:	
:	
1 k	
2 k	
3 k	
:	
:	
10 k	
20 k	
30 k	
:	
:	
100 k	
200 k	
300 k	
:	
:	
1 M	
2 M	
3 M	

CALCULATION, QUESTIONS AND DISCUSSION:

1- From your practical results, plot Vo vs the frequency on a semiology paper.
2- From the plot, determine the upper and lower cutoff frequencies.
3- Find the bandwidth.
4- Determine the gain at one octave below the upper cutoff frequency.
5- Determine the gain at one decade above lower cutoff frequency.
6- Discuss your practical results.

EXPERIMENT NO. (12)
JFET AS A CONSTANT CURRENT SOURCE

OBJECTIVE:

- To explain how FET transistor can be used as a constant current source.
- To determine the maximum RL to have a constant I_D.

THEORY:

A JFET can be used to supply constant current to a variable load by connecting its gate directly to its source as illustrated in figure 12.2. Here the resistor R_D is considered as the variable load resistance. The current that passes through R_D is independent of R_D. The condition that have to be satisfied to obtain a constant current from a JFET is:

$$|V_{DS}| \geq |V_P| - |V_{GS}| \qquad \textbf{12.1}$$

Since $V_{GS} = 0$ in the circuit shown below

$$|V_{DS}| \geq |V_P|$$

The constant current produced by JFET is then $I_D = I_{DSS}$ because $V_{GS} = 0$.

From the above condition we can find the maximum value of R_D (R_L) to have a constant current I_D.

$$|V_{DS}| \geq |V_P|$$

$$V_{DS} = V_{DD} - I_{DSS} R_L$$

$$V_{DD} - I_{DSS} R_L \geq |V_P|$$

Thus $$R_L = \frac{V_{DD} - |V_P|}{I_{DSS}} \qquad \textbf{12.2}$$

PROCEDURE:

1- Connect the circuit shown in figure 12.1.
2- Change V_{GG} until $I_D = 0$ then measure V_{GS} which equals V_P
3- Connect the circuit shown in figure 12.2.
4- For $R_D = 1k\Omega$, change V_{DD} until I_D become a constant value and then measure I_D which equals I_{DSS}.
5- Measure practically the maximum value of R_D (R_L) that keep I_D constant.

CIRUIT:

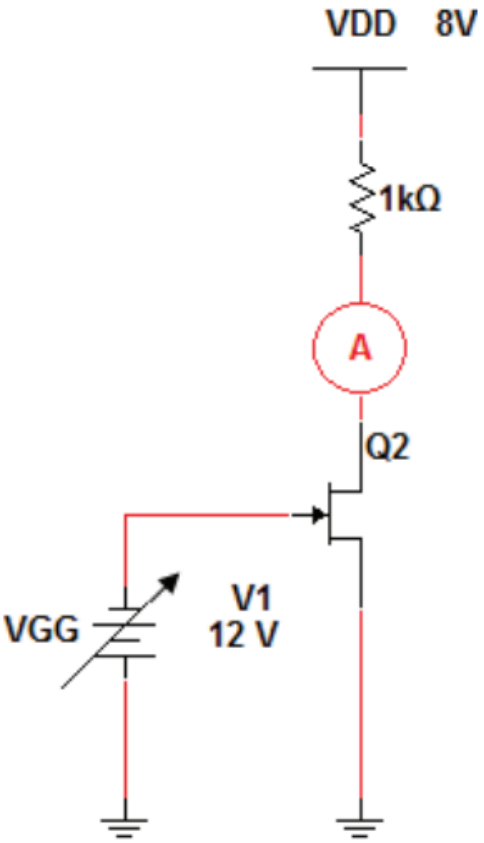


Figure 12.1

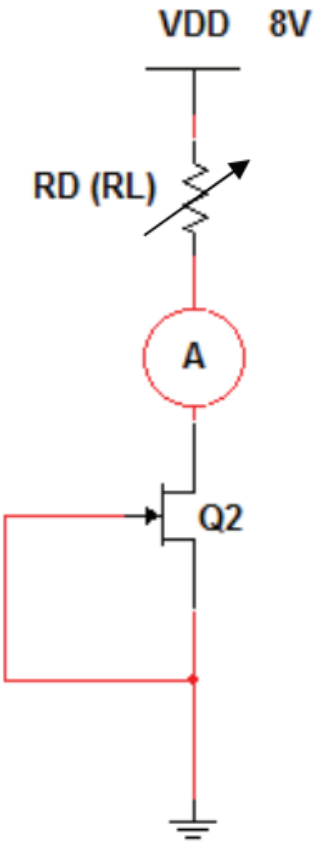


Figure 12.2

CALCULATION, QUESTIONS AND DISCUSSION:

1- Calculate the maximum value of RD (RL) that keep ID constant by using equation 12.2.
2- Discuss your results.

EXPERIMENT NO. (13)
TUNED AMPLIFIER

OBJECTIVE:

- To explain tuned amplifier.
- To explain tuned operation.
- To discuss the quality factor of a tuned amplifier.

THEORY:

Sometimes it is desired that an amplifier should be selective i.e. it should select a desired frequency or narrow band of frequencies for amplification. For instance, radio and television transmission are carried on a specific radio frequency assigned to the broadcasting station. The radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others. To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency. Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side.

In summary, the tuned amplifier only amplifies frequencies lying within a desired frequency range. This desired frequency range is selected by replacing the R_C (BJT) or R_D (FET) by a parallel resonance circuit. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at resonant frequency and very small impedance at all other frequencies.

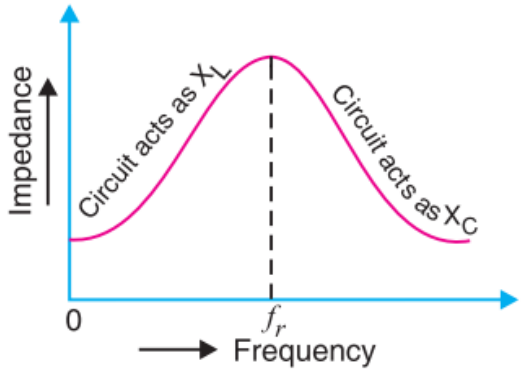


Figure 13.1

The resonance circuit impedance at the resonance frequency can be calculated as

$$Z_r = \frac{L}{RC}$$

If the input signal has the same frequency as the resonant frequency of LC circuit, large amplification will result due to high impedance of LC circuit at this frequency.

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{L - CR_L}{L}}$$

In the above equation, if R_L is neglected, the equation will be;

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

It is desired that resonance curve of a parallel tuned circuit should be as sharp as possible in order to provide selectivity. The sharp resonance curve means that impedance falls rapidly as the frequency is varied from the resonant frequency. The smaller the resistance of coil, the more sharp is the resonance curve.

$$Q = \frac{X_L}{R} = \frac{2\pi f_r L}{R} = \frac{f_r}{\Delta f}$$

$$\Delta f = BW = f_2 - f_1$$

The quality factor Q of a parallel tuned circuit is very important because the sharpness of resonance curve and hence selectivity of the circuit depends upon it. The higher the value of Q, the more selective is the tuned circuit.

CIRUIT:

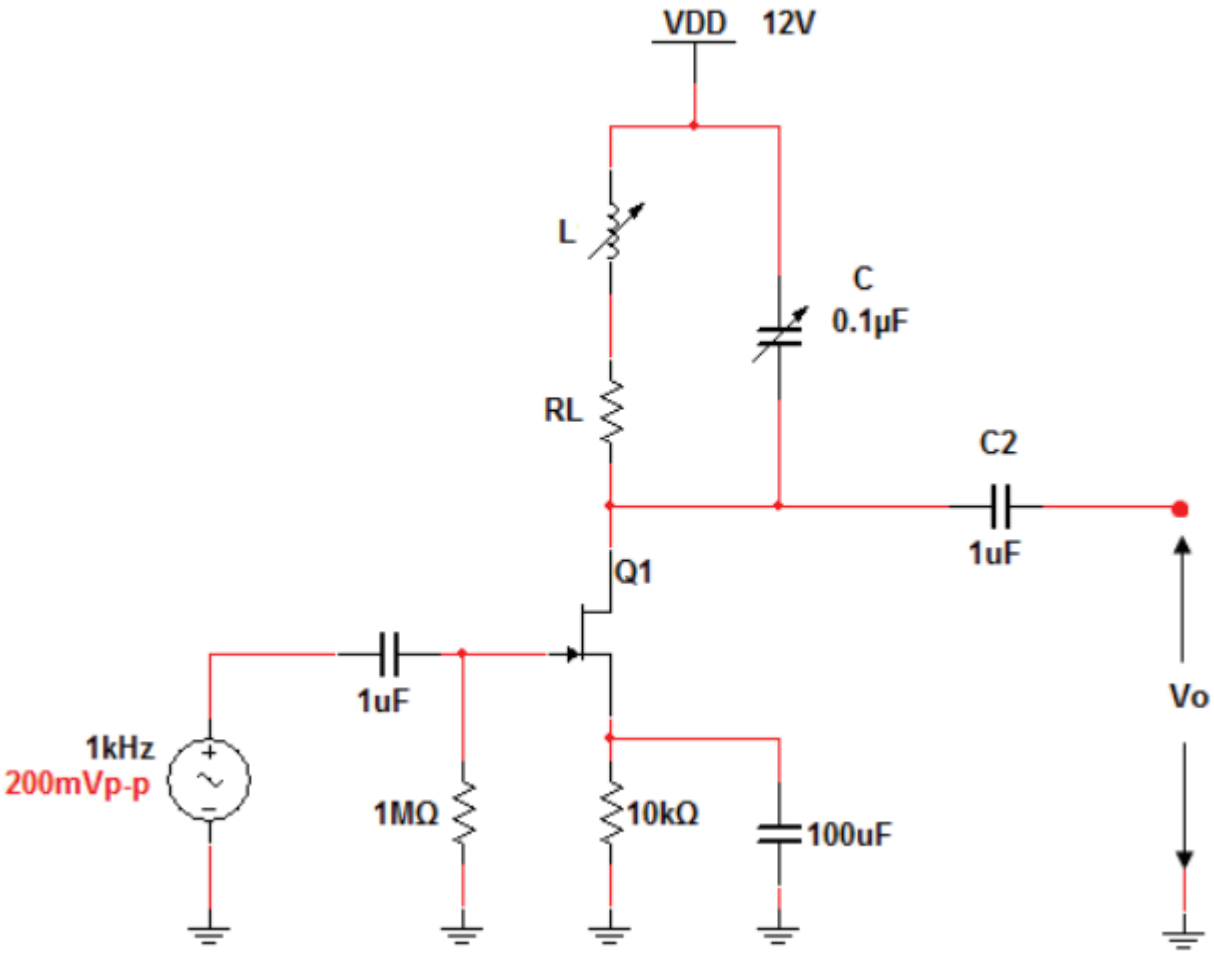


Figure 13.2

PROCEDURE:

1- Connect the circuit shown in figure 13.2.
2- Practically, determine the resonance frequency f_r for a chosen value of L.
3- Practically, measure the voltage gain for the input frequencies shown in table 13.1 when RL = 0 Ω.
4- Repeat step 3 when RL = 100 Ω (table 13.2).

When RL = 0 Ω									
$\frac{f}{f_r}$	0.5	0.6	0.8	0.9	1	1.1	1.2	1.4	1.5
Vo									
Av									

Tale 13.1

When RL = 100 Ω									
$\frac{f}{f_r}$	0.5	0.6	0.8	0.9	1	1.1	1.2	1.4	1.5
Vo									
Av									

Table 13.2

CALCULATION, QUESTIONS AND DISCUSSION:

1- Plot the relationship between Av and the input frequency (*f*).
2- Find the bandwidth from the relationship curve.
3- Find the quality (Q) of the tuned circuit.
4- Discuss your result

EXPERIMENT NO. (14)
THE DIFFERNTIAL AMPLIFIER

OBJECTIVE:

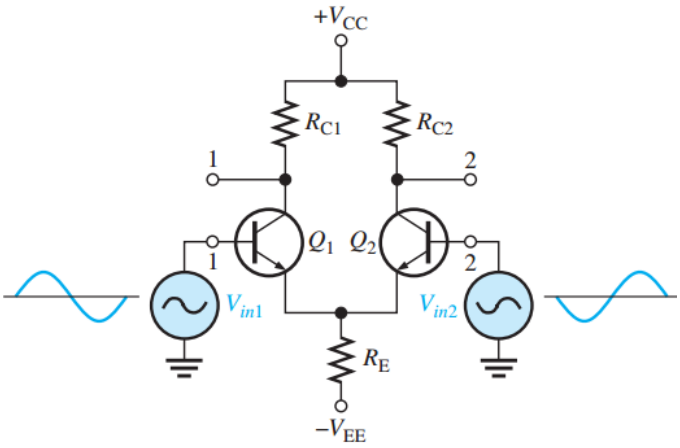
- Describe the differential amplifier and its operation.
- Calculate dc currents and voltages
- Define and determine the common-mode rejection ratio (CMRR)

THEORY:

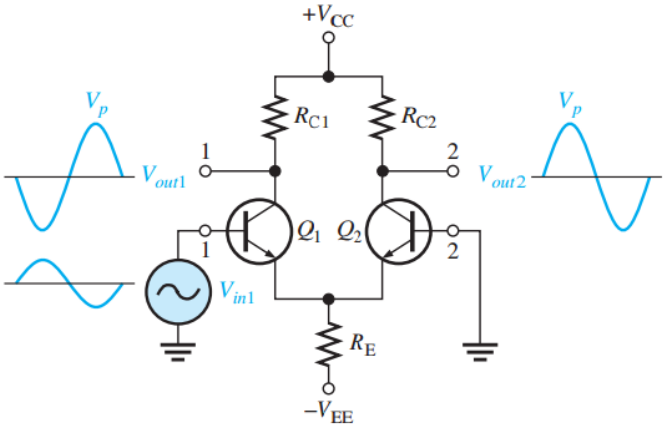
A differential amplifier is an amplifier that produces outputs that are a function of the difference between two input voltages. The differential amplifier has two basic modes of operation: differential (in which the two inputs are different) and common mode (in which the two inputs are the same).

Differential Mode;

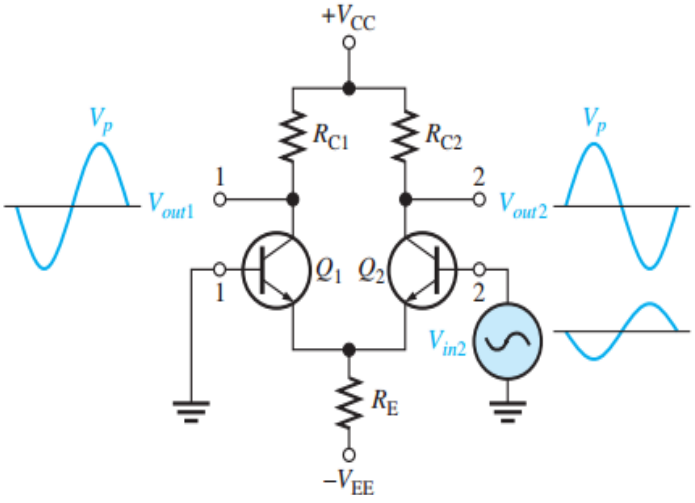
In this configuration, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in figure below.



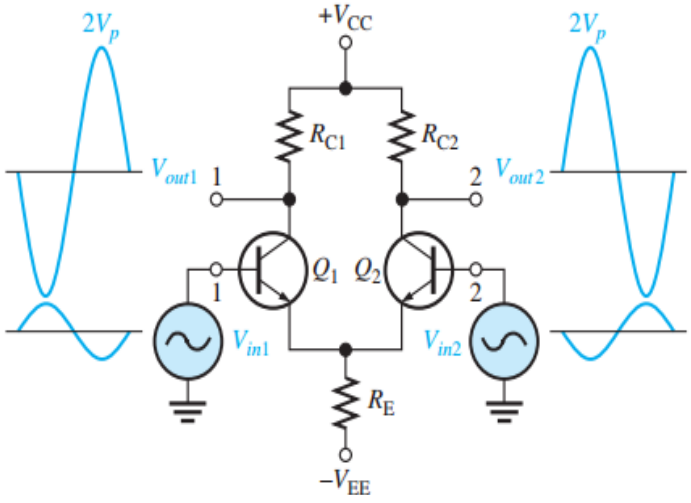
Differential inputs (180 out of phase)



The output due to V_{in1}



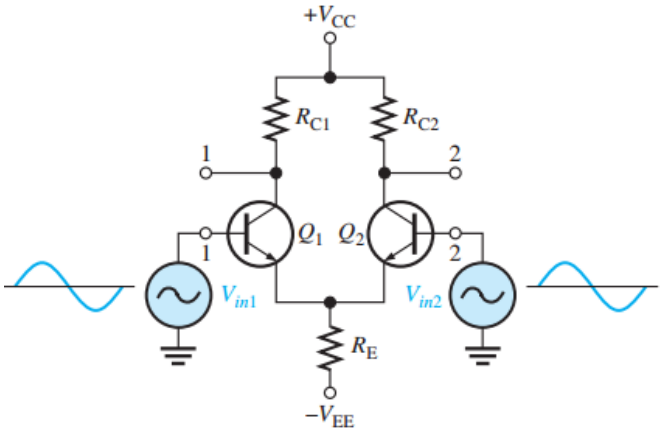
The output due to V_{in2}



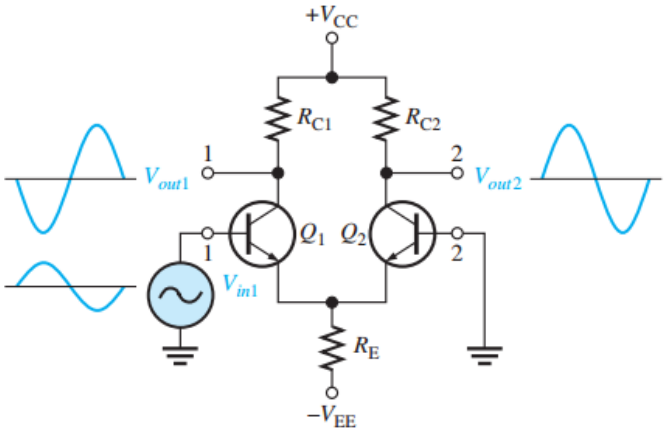
The total output due

Common Mode;

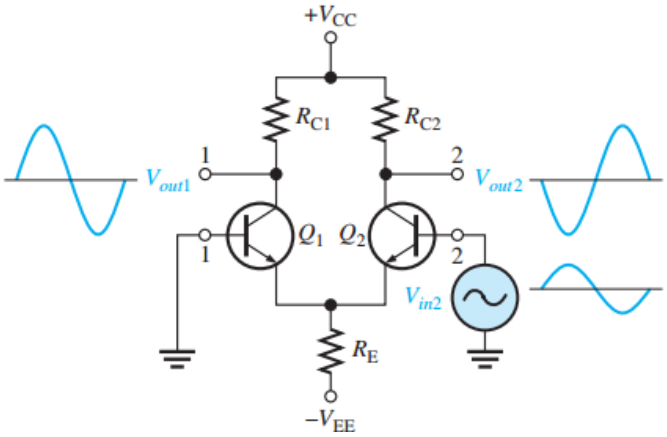
One of the most important aspects of the operation of a diff-amp can be seen by considering the common-mode condition where two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure below.



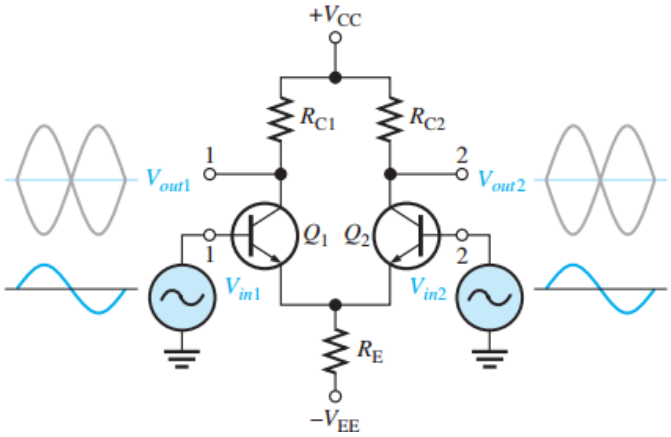
Common mode inputs (in phase)



The output due to V_{in1}



The output due to V_{in2}



Outputs due to Vin1 and Vin2 cancel because they are equal in amplitude but opposite in phase. The resulting outputs are 0 V ac.

Common-Mode Rejection Ration (CMRR);

The measure of an amplifier's ability to reject common-mode signals is a parameter called the CMRR (commonmode rejection ratio). Ideally, a diff-amp provides a very high gain for desired signals (differential mode) and zero gain for common-mode signals.

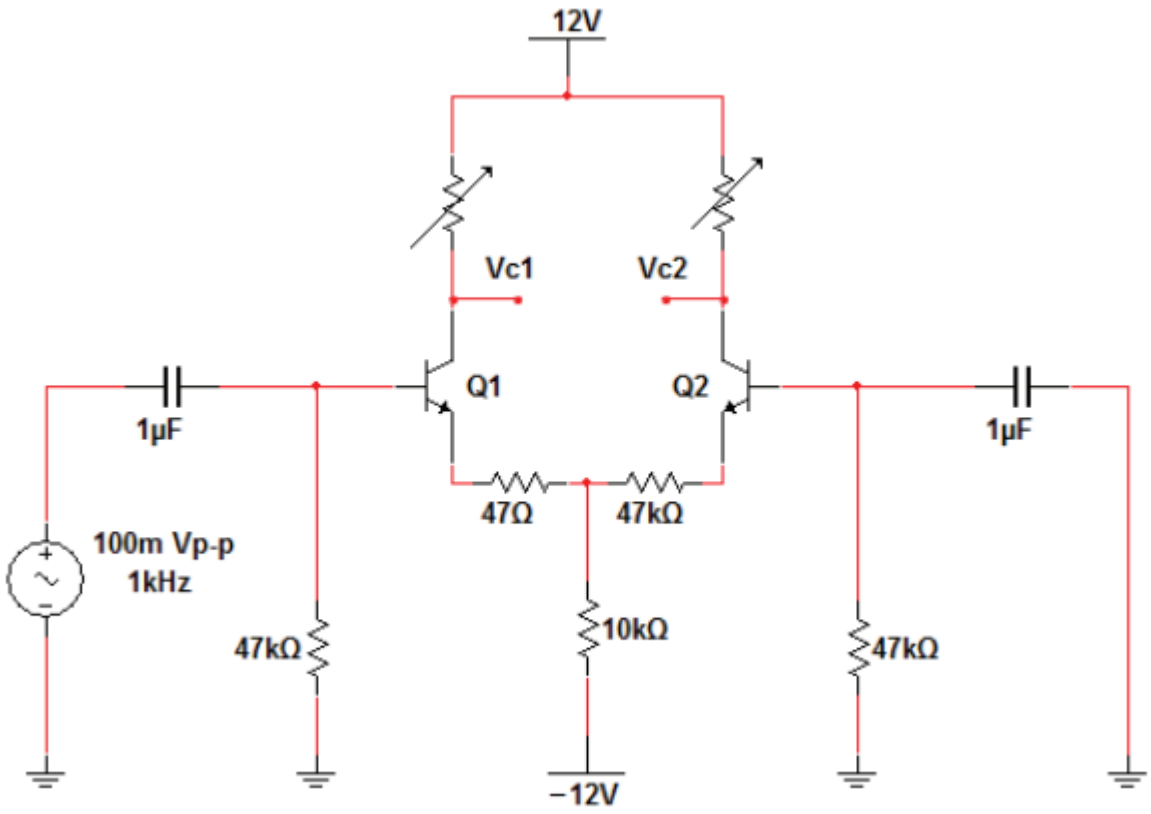
The higher the CMRR, the better. A very high value of CMRR means that the differential gain $A_{v(d)}$ is high and the common-mode gain A_{cm} is low. The CMRR is often expressed in decibels (dB) as

$$\mathbf{CMRR} = \mathbf{20 \log}\left(\frac{A_{v(d)}}{A_{cm}}\right)$$

Acm = -R_C ($2R_T$), and ***Avd = R_C / 2(R_{E2} + re)***

PROCEDURE:

1- Connect the circuit shown in figure below.



2- Set the Q-points of both transistors at the center of the dc load-line by changing R_C.
3- Practically measure the dc parameters shown in table 14.1.
4- Practically measure the ac parameters shown in table 14.2.
5- Observe V_{C1} and V_{C2} after making $V_{in1} = 0$, and $V_{in2} = Vs$.
6- Using the same source as for the two inputs, measure *Acm*.
7- Using two different source measure *Avd*.

DC parameters	Measured values	Computed Values
I_E		
I_B		
V_B		
V_E		
V_A		
V_C		

Table 14.1

DC parameters	Measured values	Computed Values
I_E		
I_B		
V_B		
V_E		
V_A		
V_C		

Table 14.2

CALCULATION, QUESTIONS AND DISCUSSION:

1- Compute the dc parameters theoretically and compare them with the measured values in table 14.1.
2- Compute the ac parameters theoretically and compare them with the measured values in table 14.1.
3- Discuss Your results

EXPERIMENT NO. (15)
LOGIC GATES

OBJECTIVE:

- Explain how to use diode to build OR and AND gates.
- Explain how to use transistor to build invertor, NOR and NAND gates.
- Describe the saturation and cutoff regions of a transistor.

THEORY:

A gate is a logic circuit with one output and one or more inputs. An output occurs only for a certain combinations of input signals. Logic gates are digital (two states) circuits because the input and the output signals are either high or low voltages. Gates cab be described with Boolean algebra.

A diode is like an electronic switch. When a diode is forward biased and a required forward voltage is applied, the diode is on (switch is on). However, when zero voltage or a revered biased voltage is applied the diode is off (switch is off). This characteristic of the diode is very useful to build logic gate such as OR and AND gates.

In a transistor, the collector-to-emitter impedance is quite low near or at saturation and large near or at cutoff. For instance, the load line defines *saturation* as the point where the current is quite high and the collector-to-emitter voltage quite low as shown in Figure 15.1. At *cutoff*, the current is relatively low and the voltage near its maximum value.

The above impedance levels established by "on" and "off" transistors make it relatively easy to understand the operation of the logic gates.

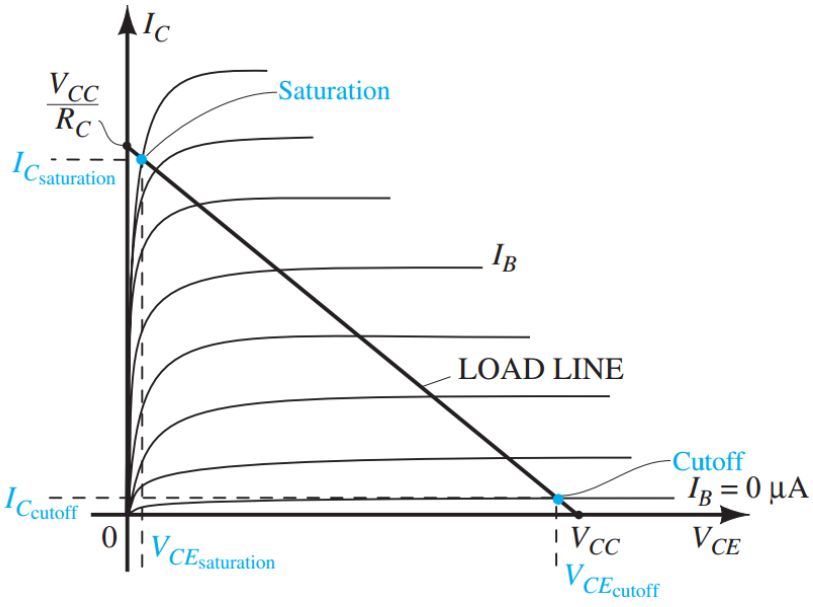


Figure 15.1 Points of operation for a BJT logic gate.

THE LOGIC GATES:

1- **Invertor:** An investor is a gate with only one input and one output. The output state is always the opposite of the input state.

The logic symbol of the invertor

2- **OR gate:** The OR gate has two or more inputs, but it has only one output. If any input is high the output is high.

The logic symbol of a two input OR gate

3- **AND gate:** The AND gate has two or more inputs, but it has only one output. All inputs must be high to get a high output.

The logic symbol of a two input AND gate

THE CIRCUITS:

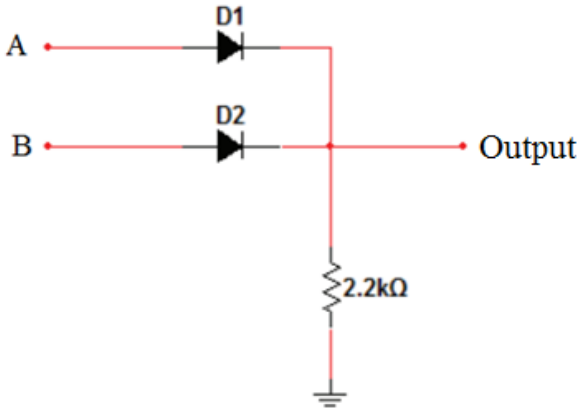


Figure 15.2 OR gate

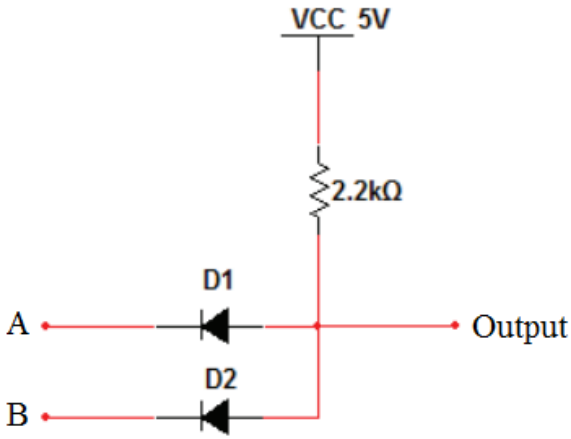


Figure 15.3 AND gate

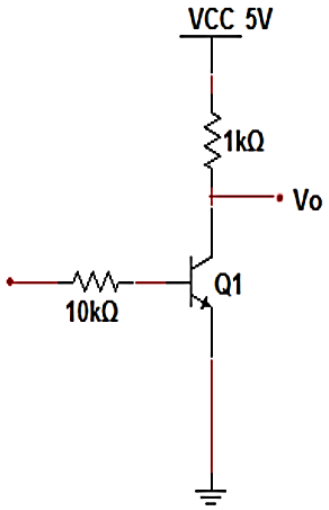


Figure 15.4 Inverstor

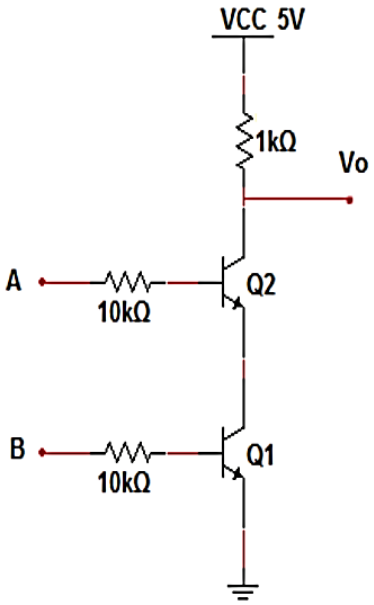


Figure 15.5 NAND gate

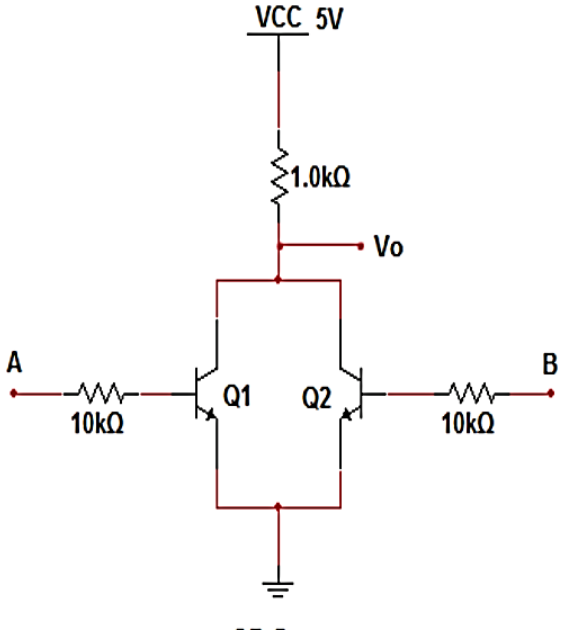


Figure 15.6 NOR gate

PROCEDURE:

1- Connect the circuit shown in figure 15.2

2- Write the truth table of the circuit.

A	B	OUTPUT

3- Connect the circuit shown in figure 15.3

4- Write the truth table of the circuit.

A	B	OUTPUT

5- Connect the circuit shown in figure 15.4

6- Write the truth table of the circuit.

INPUT	OUTPUT

7- Connect the circuit shown in figure 15.5

8- Write the truth table of the circuit.

A	B	OUTPUT

9- Connect the circuit shown in figure 15.6

10- Write the truth table of the circuit.

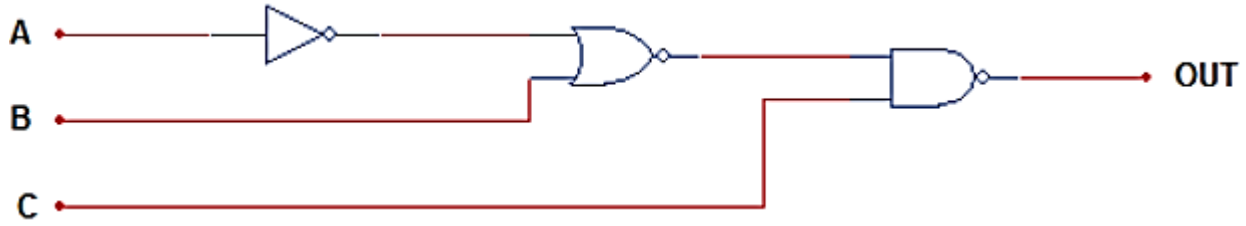
A	B	OUTPUT

CALCULATION, QUESTIONS AND DISCUSSION:

1- Design an OR gate using transistors only.

2- Design an AND gate using transistors only.

3- Design the circuit shown below using transistors only.



4- Discuss your results.

EXPERIMENT NO. (16)
LINEAR OPRATIONAL AMPLIFIER (OP-AMP) CIRCUIT

OBJECTIVE:

- Become familiar with operational amplifier circuits.
- To study operational amplifier (op-amp).
- To study inverting and non-inverting amplifiers.

OPERATIONAL AMPLIFIER:

The standard operational amplifier (op-amp) symbol is shown in Figure 16–1(a). It has two input terminals, the inverting (-) input and the non-inverting (+) input, and one output terminal. Most op-amps operate with two dc supply voltages, one positive and the other negative, as shown in Figure 16–1(b), although some have a single dc supply. Usually these dc voltage terminals are left off the schematic symbol for simplicity but are understood to be there.

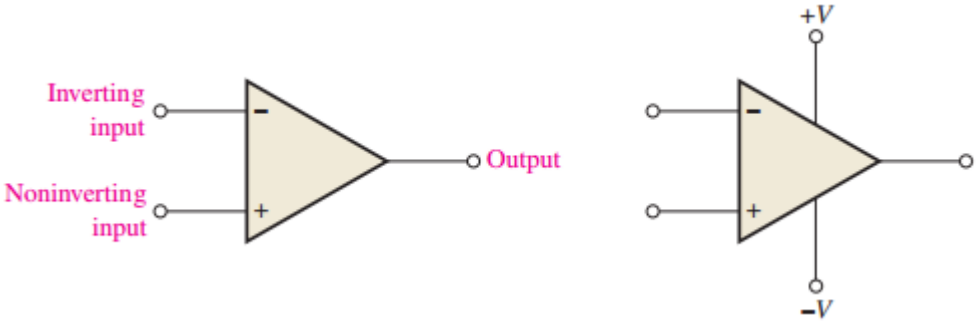


Figure 16.1 (a) Symbol (b) Symbol with dc supply connections

The ideal op-amp has *infinite voltage gain* and *infinite bandwidth*. Also, it has an *infinite input impedance (open)* so that it does not load the driving source. Finally, it has a *zero output impedance.* Although integrated circuit (IC) op-amps approach parameter values that can be treated as ideal in many cases, the ideal device can never be made. Characteristics of a practical op-amp are *very high voltage gain, very high input impedance, and very low output impedance.*

Inverting Amplifier:

An op-amp connected as an inverting amplifier with a controlled amount of voltage gain is shown in Figure 16–2. The input signal is applied through a series input resistor Ri to the inverting input. Also, the output is fed back through Rf to the same input. The non-inverting (+) input is grounded.

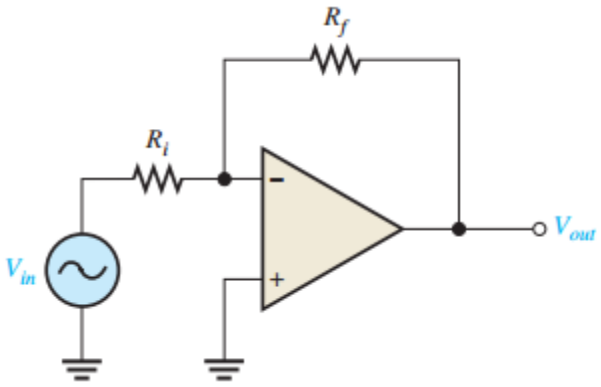


Figure 6.2 Inverting Amplifier

Since there is no current at the inverting input, the current through Ri and the current through Rf are equal.

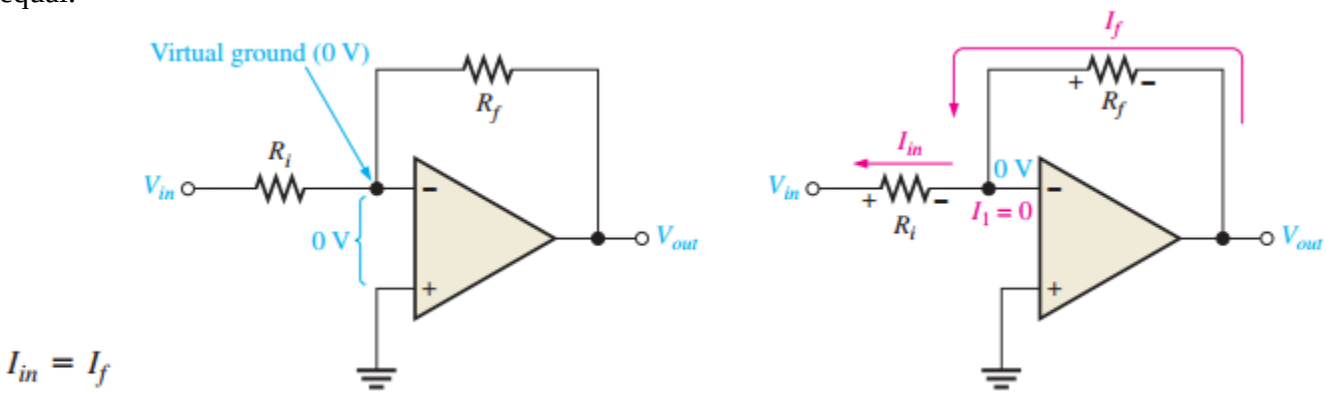


Figure 16.3 (a) Virtual ground (b) $I_{in} = I_f$ and current at the inverting input (I_1) is 0

The voltage across *Ri* equals *Vin* because the resistor is connected to virtual ground at the inverting input of the op-amp. Therefore,

$$I_{in} = \frac{V_{in}}{R_i}$$

Also, the voltage across R_f equals because of virtual ground, and therefore

$$I_f = \frac{-V_{out}}{R_f}$$

Since $I_f = I_{in}$

$$\frac{-V_{out}}{R_f} = \frac{V_{in}}{R_i}$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

Of course, Vout/Vin is the overall gain of the inverting (I) amplifier.

$$A_{cl(I)} = -\frac{R_f}{R_i}$$

Non-inverting Amplifier:

An op-amp connected in a closed-loop configuration as a non-inverting amplifier with a controlled amount of voltage gain is shown in Figure 15–4. The input signal is applied to the non-inverting (+) input. The output is applied back to the inverting input through the feedback circuit (closed loop) formed by the input resistor Ri and the feedback resistor Rf. This creates negative feedback as follows. Resistors Ri and Rf form a voltage-divider circuit, which reduces Vout and connects the reduced voltage Vf to the inverting input. The feedback voltage is expressed as,

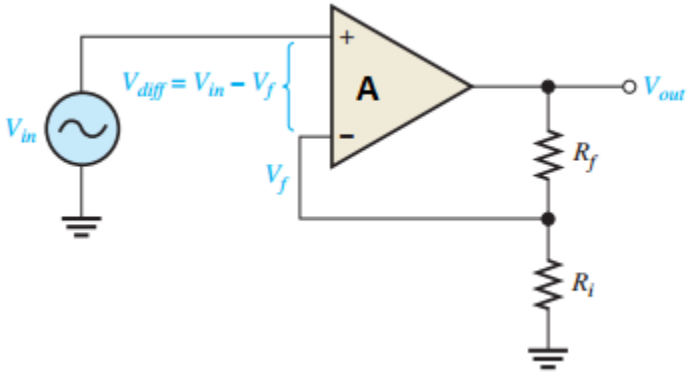


Figure 16.4 Non-inverting Amplifier

$$V_{out} = A(V_{in} - V_f)$$

$$V_f = \frac{R_i}{R_i + R_f} V_{out}$$

$$V_{out} = A\left(V_{in} - \frac{R_i}{R_i + R_f} V_{out}\right)$$

$$V_{out} = AV_{in} - \frac{R_i}{R_i + R_f} A V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{\left(1 + \frac{R_i}{R_i + R_f} A\right)}$$

The product $\frac{R_i}{R_i + R_f} A$ is typically much greater than 1, so the equation simplifies to

$$A_{overall} = \frac{R_i + R_f}{R_i}$$

CIRCUITS:

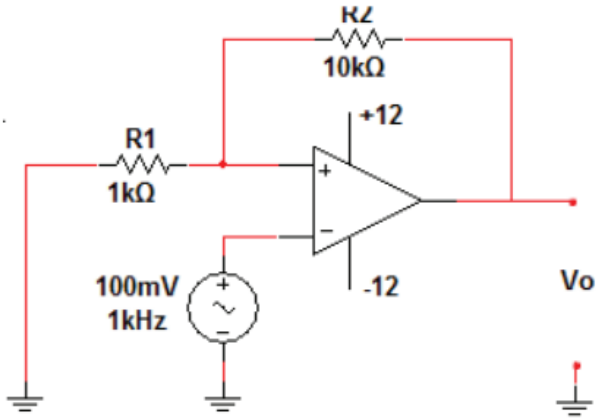


Figure 16.5 Inverting Amplifier

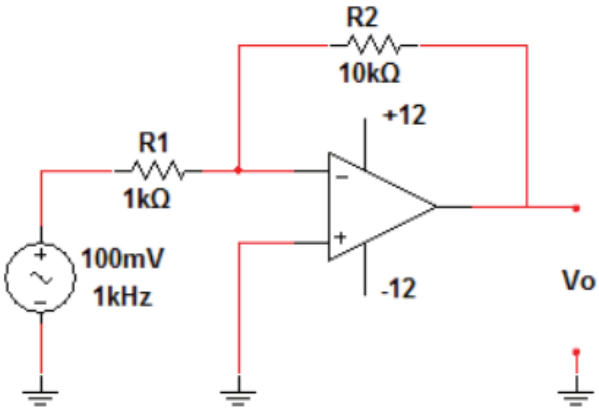


Figure 16.6 Non-inverting Amplifier

PROCEDURE:

1- Connect the circuit shown in fig. (16.5).
2- Measure the output voltage.
3- Determine the input impedance of the OP-AMP
4- Connect the circuit shown in fig. (16.6)
5- Measure the output voltage.
6- Determine the output impedance of the OP-AMP.

CALCULATION, QUESTIONS AND DISCUSSION:

1- Compute theoretically the voltage gain of the two circuits and compares it with the measured values.
2- Discuss your results

EXPERIMENT NO. (17)
ASTABLE MULTIVIBRATOR

OBJECTIVE:

- To study the characteristics of the astable multivibrator.
- To study the use of the astable as a voltage to frequency converter.

THEORY:

The astable multivibrator has two quasi – stable states and periodic transition occur from one state to the other. As shown in figure (17.1) one state is with the transistor T2 nonconducting whereas the other state is the reverse of this. The output square wave contains a large number of frequencies, hence the name multivibrator. If R1 = R4, R2=R3=R and C1=C2=C, the circuit is said to be symmetrical and each transistor remains in conducting state for the same time. In this case, the mark- to –space ratio is unity and the time period T of the oscillator is given approximately by:

T=1.4 RC seconds ……. (1) where R is in ohms, C in farads.

F = 1/T (HZ) ……..... (2)

The frequency of oscillation may be varied over the range from cycles to megacycles per seconds by adjusting R or C. It is also possible to change T electrically by connecting R2 , R3 , to an auxiliary voltage according to the equation;

T = 2RC ln (1+Vcc/V) …… (3)

Such a circuit is called voltage to frequency converter it is shown in figure (17.2)

PROCEDURE:

1- Connect the circuit of figure (17.1) and draw the wave forms of V_{B1}, V_{B2}, V_{C1}, V_{C2} respectively with all required indications.
2- Repeat step 1 for values of $R_2 = 22k\Omega$, $R_3 = 47k\Omega$, $C_1 = C_2 = 0.1\mu F$.
3- Connect the circuit of figure (17.2) and change the applied voltage (E) from 1 to 6 volt in suitable steps (say 0.5 volt), and observe the output voltage Vo and measure T corresponding to each step.

E volt	Vo	T

CALCULATION, QUESTIONS AND DISCUSSION:

1- Try to show the principle of operation of each circuit and discuss the outputs of the circuit and then conclude yours by comparing the theoretical and experimental results.
2- Derive equations 1 and 3.

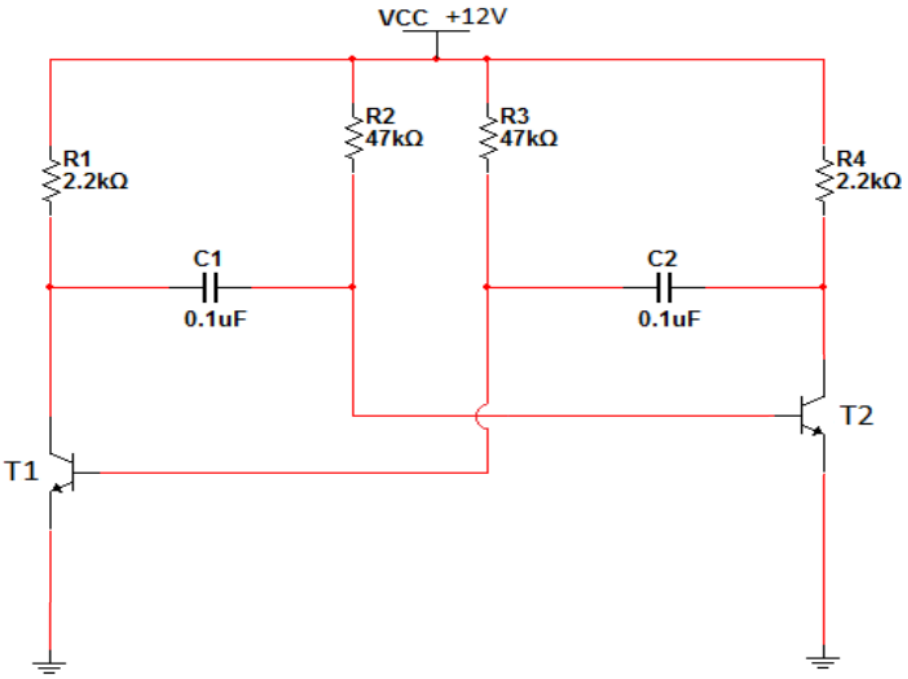


Figure 17.1

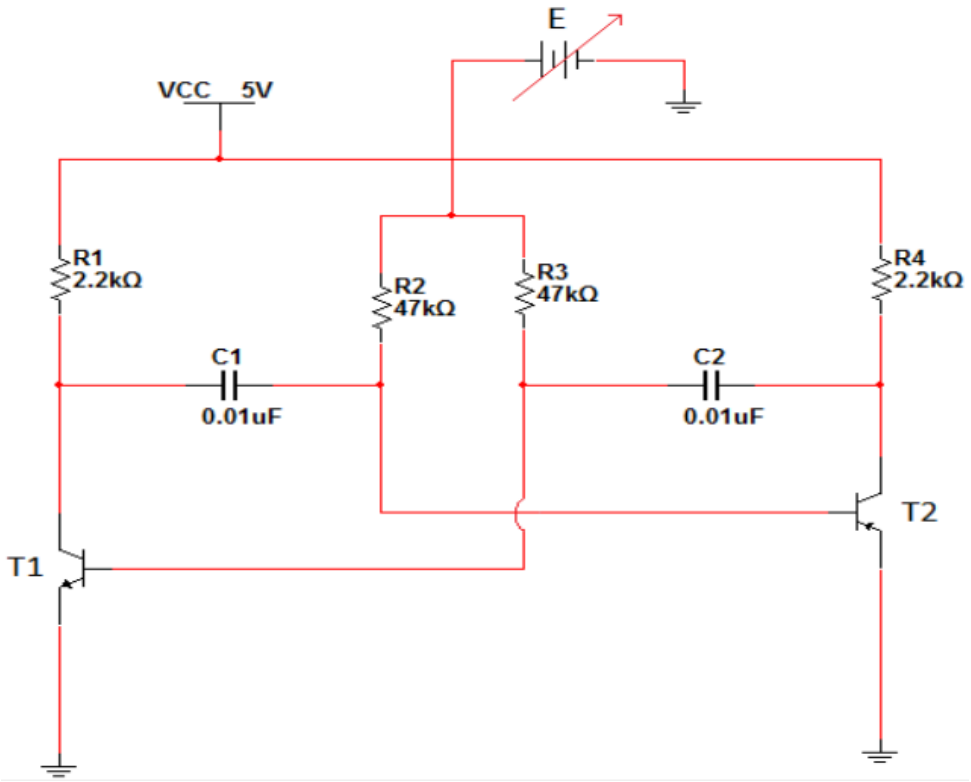


Figure 17.2