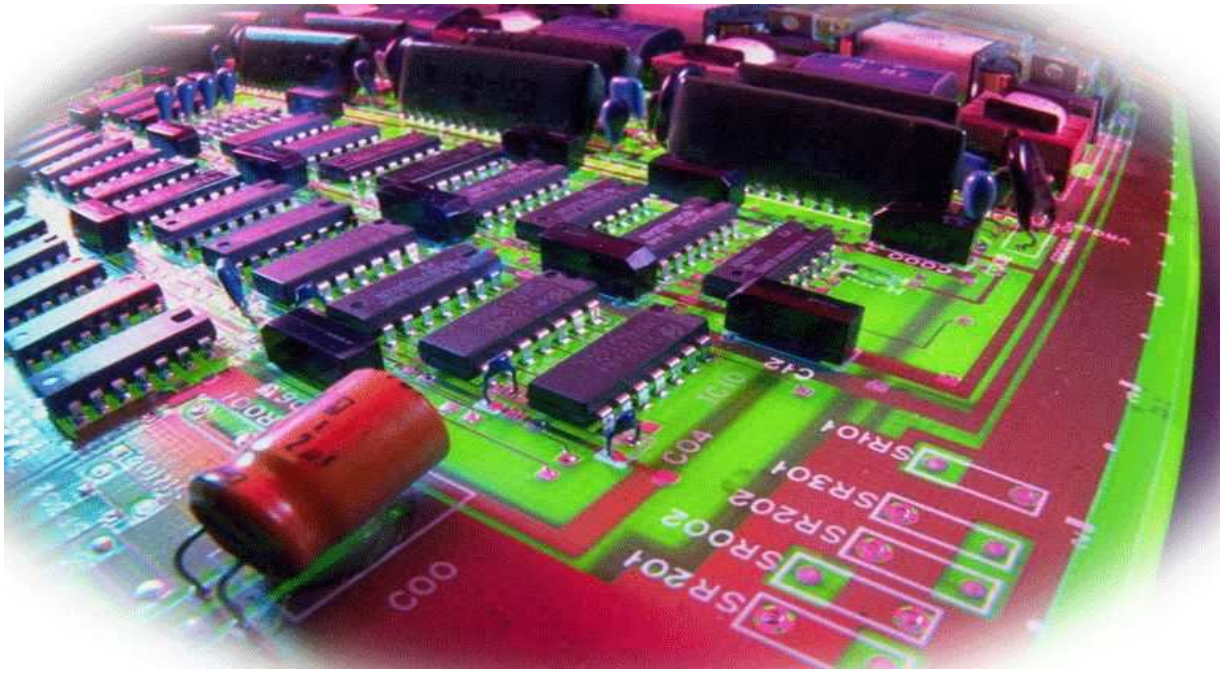
Salahaddin University

College Of Engineering

Electrical Department

Electronics Laboratory

Manual of Electronics Laboratory



Dedication:

Dedicate To all Students in Electrical Engineering Department.

Table of Contents:

EXPERIMENT NO. (1)
POWER SUPPLY
VOLTAGE REGULTOR

Theory:

A DC voltage regulator maintains a constant output voltage in dependent of changes in external load RL or changes in input voltage. The most common arrangement is the series regulator with voltage negative feedback fig (1-1).

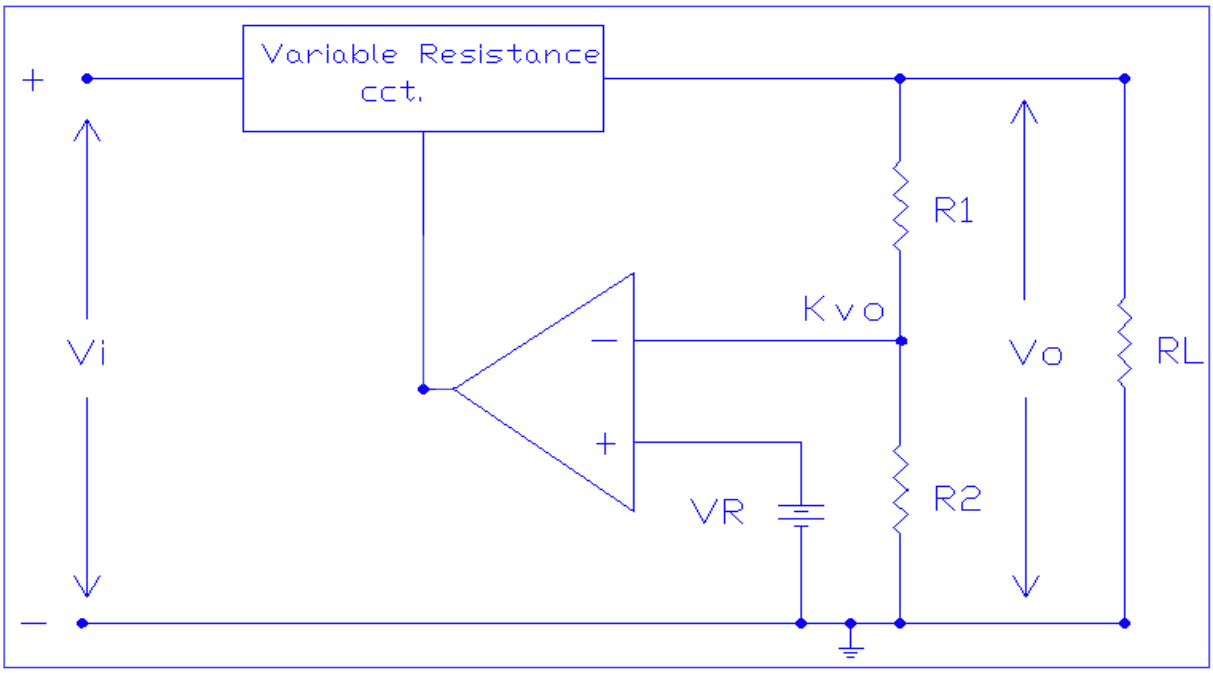


Fig (1-1)

The variable resistance is an active device usually a power transistor operating in CC config. The amplifier compares the reference voltage VR & feedback voltage Kvo. If Vo changes the difference signal VR- Kvo is amplified &applied to the variable resistance cct. Which changes its resistance & brings Vo back to the correct value thus the change input voltage Vi is balanced by change of voltage drop across the variable resistance cct.

Vo = K *AV, where AV is the voltage gain. The change of the o/p is very small.
ΔVi = ΔVo +ΔVo KAV or
ΔVi = ΔVo +ΔVo (1+KAV)
The quality factor of the cct. Is defined by the Sv:
Sv = ΔVo/Δvi = 1/ (1+KAV)

The detail of cct. Is shown in fig (1-2).The same cct. Being diagrammed in different ways is presented in fig. (1-3). In such a presentation, the CE differential signal amplifier (T1) & the CC variable resistance stage (T2) are easy to identify.

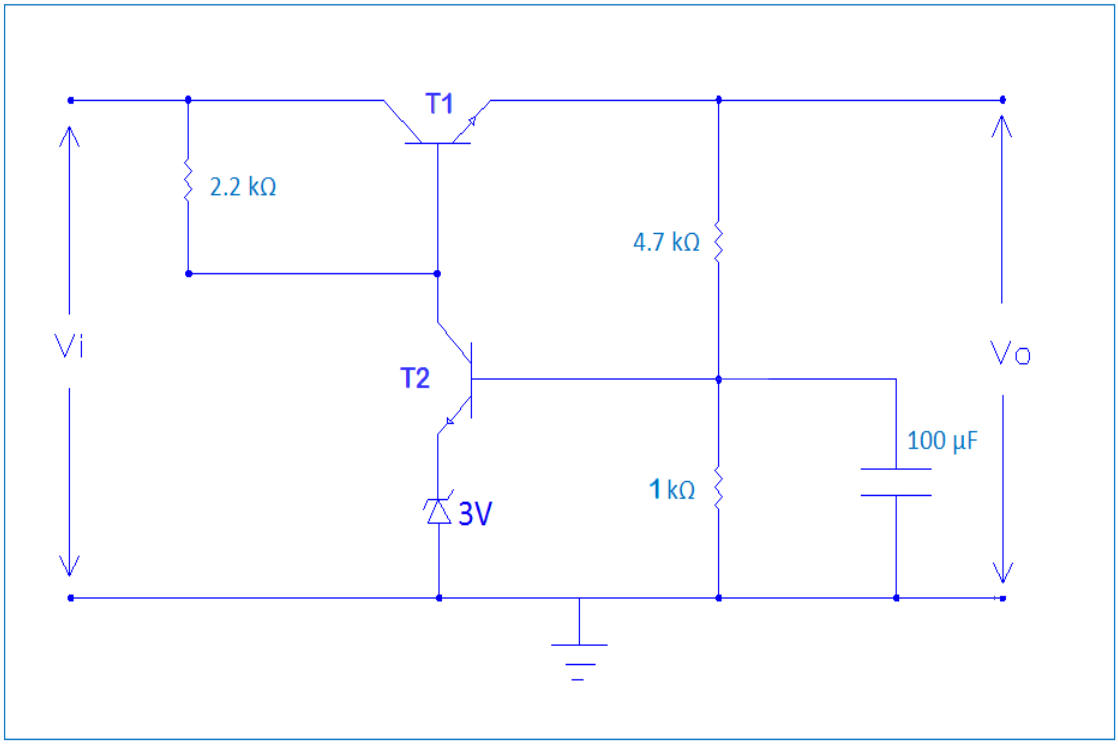

T1
2.2 kΩ
4.7 kΩ
Vi
T2
Vo
100 µF
1 kΩ
3V

Fig (1-2)

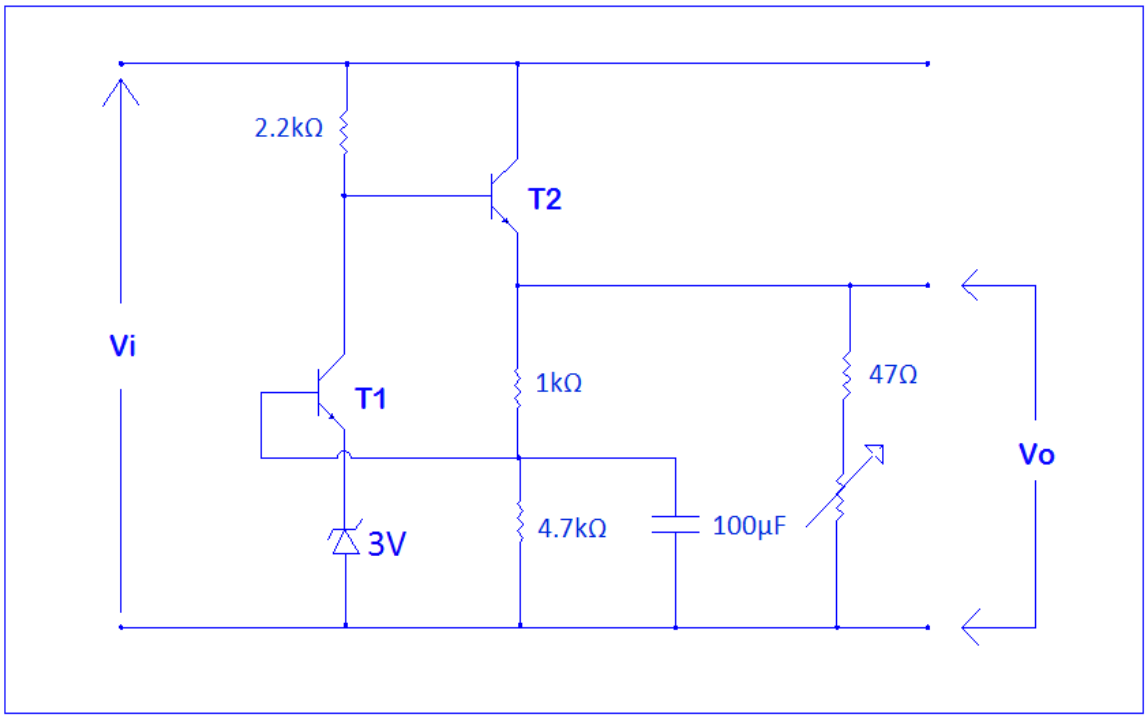

2.2kΩ
T2
Vi
T1
1kΩ
47Ω
Vo
3V
4.7kΩ
100µF

Fig (2-3)

b. Assemble the measurements set as shown below.

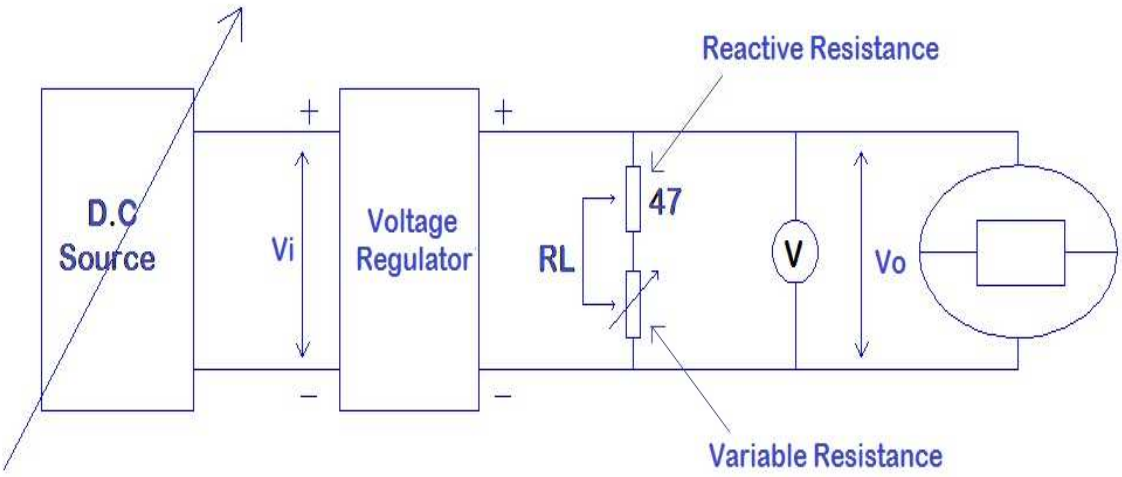


Fig (1-4)

c. Using the oscilloscope, check the cct. Performance (no AC should be observed at the o/p).
d. Measure the regulation characteristics for the values of load resistance given in the table below:

Vi(V)	1	2	3	4	5	6	7	8	9	10
Vo(V) for RL = 47										
Vo(V) for RL = 75										
Vo(V) for RL =100										
Vo(V) for RL =150										
Vo(V) for RL =200										

Home work:

1. Plot the set of regulation characteristics Vo = F(Vi) for Rl = (47,75,200)
2. Plot the set load characteristics Vo = F(Io) where Io = Vo/RL for Vi = (3,6,10) V.
3. Determine the regulation factor Sv in operation range.
4. Answer the following questions:

a. Why the regulation works properly only after Vi is greater than some specific value?
b. What is the condition of the (T1) before this value is maintained.
c. How the circuit should be modified to obtain another value of regulated o/p?

EXPERIMENT NO. (2)
TRANSISTORS AS A SWITCH

Objective:

To study the characteristics of Bipoler junction transistor & junction FET when operated as switch.

Theory:

1. *The BJT as a switch:* The BJT can be operated as a controlled switch that is the switch terminals are controlled by a signal at the third terminal. In addition the BJT current gain allows a small i/p current to control a large switch current. When used as a switch the transistor operates in either the ON region or in OFF region and switches between the two .In the ON region the transistor acts as a very low resistance between collector & emitter (typically 1 – 50 Ω) in the OFF region the transistor acts as a very high resistance between collector & emitter (typically 10 MΩ) . The transistor can be visualized as a perfect switch as shown in Fig (2 – 1). In analyzing switching ccts a simple approximate method instead of using transistor curves is used as illustrated.

   A) The ON condition: In Fig. No. (2 – 2) the transistor will operate in ON state when a positive Vi is applied to the cct to produce sufficient base current to saturate the transistor , the I can be evaluated as :

   $$I_{B\,min} = (V_i - V_{BE}) / R_B \quad \ldots\ldots\ldots\ldots (1)$$

   And $I_c = h_{fe} * I_B$ in active region

   When the transistor is fully saturated Ic will be :

   $$I_{c(sat)} = V_{cc}/R_c \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

   As IB is increased from zero , the collector current increase proportionally until it reaches Ic (sat) where further increase in IB will not produce an increase in Ic which is saturated at the value Ic (sat). the value of base current IB that will cause saturation can be determined by :

   $$I_{B(sat)} = I_{c(sat)} / h_{fe} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

   B) The OFF condition : the transistor will be OFF whenever IB = 0 , In this case only a small leakage current will flow in the collector & emitter which can be neglected & all of Vcc appears across the collector & emitter.

2. *The JFET as a switch :* Fig (2-3) shows an N-channel JFET connected in the common source configuration when its to be operated as a switch the JFET input VGS has to switch between 0 V (which will put the transistor in ON state) &VGS (OFF) (the required voltage to put the transistor in OFF state).

   The drain source resistance (rds in ON state typically ranges from 10 -100 ohm, while rds (OFF) is typically 1000 M ohms or more. In JFET transistors the VGS (not current) that determines whether the resistance between the switch terminals (Drain & Source) will be low or high .one of the major advantages of JFET transistor switch over the BJT switch that draws negligible current from the input signal . A disadvantage of JFET switch is that the gate input voltage has to have a polarity opposite to that of the drain voltage. Thus the output from JFET switching ccts cannot directly drive the input of another.

3. *Transistor switching times :* to see the behavior of transistor as it makes a transition from on state to off state or vice versa consider the switch of fig (2-2) driven by a pulse this wave form makes transition between voltage level V & V at Voff the transistor is at cutoff & at Von the transistor is in saturation . The response of the collector voltage to the input is shown in fig (2-4). When the input jumps to V1 in order to turn the transistor on the charged junction capacitances (Cbe , Cbc) cause a delay the output takes time to go from VCC volt to Zero volts & the time that it takes the output to

drop by 10 % is called delay time(td) the time it takes the output to drop an additional 80 % is called the fall time (tf) the sum td + tf is called the turn ON time (T ON). When the input drops to V2 in order to turn transistor OFF once again the junction capacitance cause a delay in the transition when the transistor is saturated any base current above IB (sat) dose not produce an increase in Ic as a result is an excess of charges stored in the base region when the input tries to turn the transistor OFF the excess charges in the base are still available to produce collector current .As a result collector saturation current keeps flowing until the excess base charges are completely removed . This time interval is called the storage time (ts) after the end of storage interval the transistor can not turn OFF completely until Ccb charges to (VCC + V2) through Rc eventually the transistor ends up in the OFF state the total turn OFF time (t off) is the sum of ts & tr.

Speed – Up capacitors: The faster (t on) requires a small (RB) while a faster (t off) requires a large value of (RB) . This problem can be solved by using speed – up capacitors across (RB).

Over drive factor: is the ratio of the base current to the minimum base current required to put the transistor in saturation.

Procedure:

1 – Connect the circuit shown in Fig (2-2) with Rc = 2.2 K, Rb = 10 K and 2SC945 transistor.

2 – Find transfer characteristics (V_{cE} versus Vi) by applying an input voltage from (-5 to +5 volt in suitable steps) , increase the measurement in the active region .

3- Measure the voltage (VBE) required for saturation.

4- Apply a square wave of frequency 100 KHZ and 10 (V_{p-p}) to the input and draw the out put waveform under the input (together with the time relationship) and measure the switching times.

5- Decrease the input voltage to 6(V_{p-p}) and observe the switching times, if there is any changes then record your observations.

6- Connect a (720) PF capacitor in parallel with R_B and study its effect on the switching times.

7- Repeat steps (1-5) for the circuit of FIG (2-3) with R_D = 10 K ohms.

Questions:

1- Measure the minimum base current required for saturation theoretically.

2- Measure the over drive factor when the input is 10 volts.

3- Discuss the effects of R_B and R_C on the value of (t_{ON})

4- Discuss how to change R_B and R_C so as to reduce (t_{off}).

5- Why the output of a JFET switch cannot drive the input of another JFET switch?

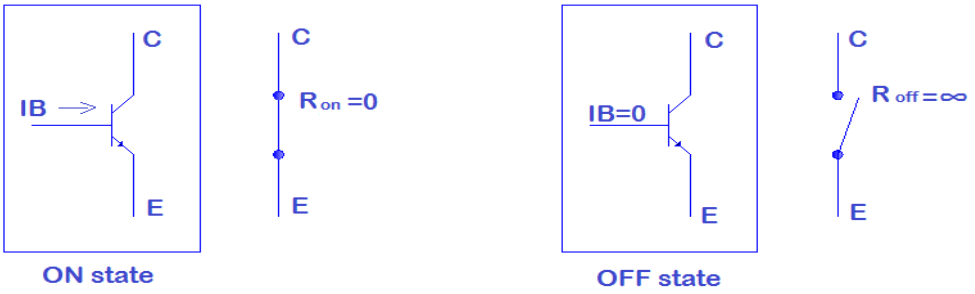


Fig (2-1)

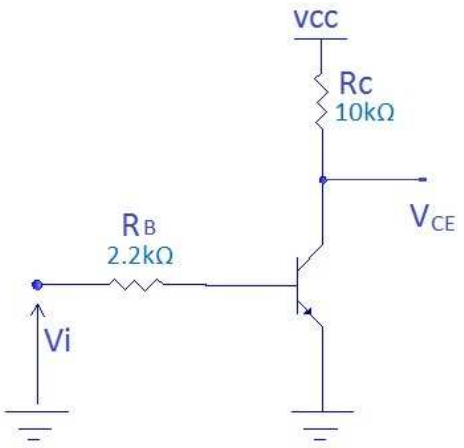


Fig (2-2)

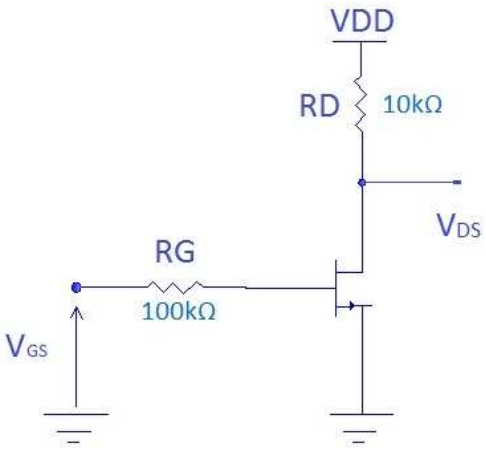


Fig (2-3)

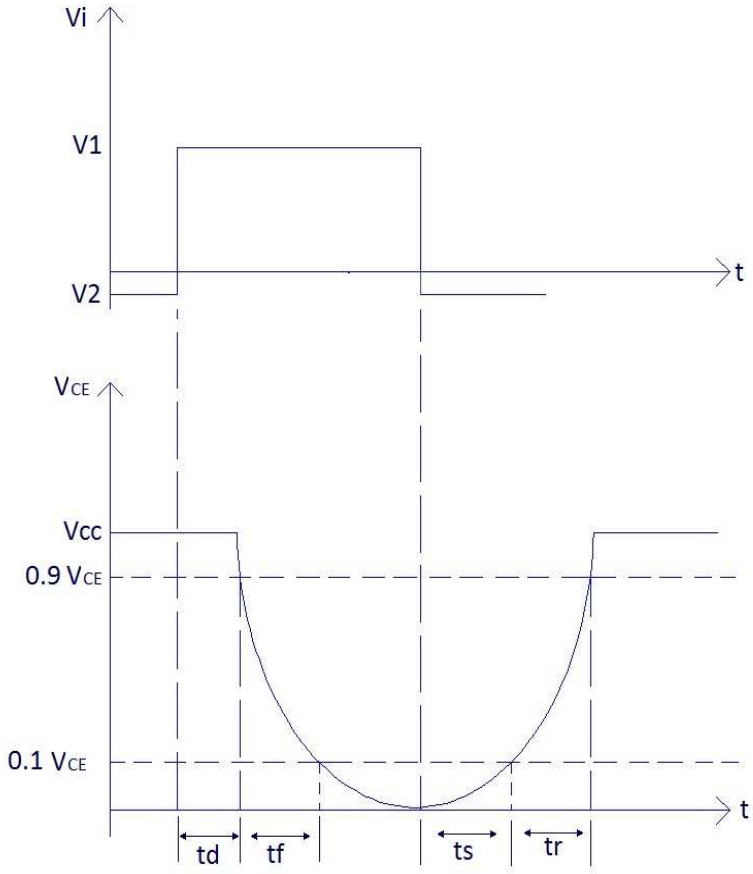


Fig (2-4)

EXPERIMENT NO. (3)
BISTABLE MULTIVIBRATOR

Objective:

To study the bistable multivibrator and familiar with the circuit inner voltage and triggering methods.

Theory:

The bistable is a circuit, which can exist infinitely in either of two stable states and where an abrupt transition from one state to the other can be induced by means of some external excitation usually in form of an input pulse. It is used extensively for counting and for storing binary information .The basic circuit shown in FIG(3-1) is a two stage amplifier with direct coupling between the stages, the circuit operates as follows, consider a small voltages fluctuation at the base of Ti this fluctuation will be amplified and fed in an inverted state to the base of T2 where it is further amplified by T2 and inverted to be positive feedback to the base of T1 where the original voltage fluctuation is augmented.
This feedback will ensure that one of the transistor is driven in to saturation while the other is cut. The cct. Will remain in this stable state until an input pulse initiates the transition. There are many applications of the bistable (flip-flop) in which desired to have a change of state as soon as a triggering signal is applied . The transition time is defined as the interval during which condition transfers from one transistor to the other, this time can be reduced by shunting coupling transistors with a small capacitors (speed-up capacitor). After the transition an additional time is required for reaching the capacitors C1,C2 to their new voltages, this additional time called SETTLING TIME. A transition having been induced by triggering signal, a certain minimum time must elapse before a succeeding trigger will be able reliably to in induce the reverse state. The smallest allowable interval between triggers is called the resolving time of the flip-flop, and its reciprocal is the maximum frequency at which the flip-flop will respond, also this time is the sum of the transition time and the settling time of the circuit.

If the storage, delay, rise and fall times are small compared with the settling time of the circuit. The flip-flop can be triggered reliably by maximum frequency of (Fmax.) given by:

Fmax. = 1/2t = (R1 +R2)/(2*C*R1*R2)
Where t is the time constant iof the Rc circuit and is given by:
T=(R1*R2*C1)/(R1+R2)

Equipment: The equipment required are:

Two BJT transistor (2SC945) , multivalve resistors, diodes and power supply.

Procedure:

1- Connect the circuit shown in FIG (3-1) and measure the voltages at V_{CE1}, V_{CE2}, V_{BE1}, V_{BE2}, in the cases that base1, base 2 are (O.E, OO, E.O, O.O, E.E) respectively where: E = earth, O = open.
2- Connect the cct. Of FIG (3-2) and apply a negative going (square wave). Triggering signal observe and record the wave forms of VCE1, VCE2 try sinusoidal and triangular wave forms for triggering, what will be the output?
3- With the same circuit measure the max. frequency at which the bitable will switch reliably and hence calculate the resolving time ($t_{resolv} = t_{sett} + t_{trans}$)
4- Replace the resistors Rc1, Rc2 with 100 ohm resistors and connect in series with it a LED and apply a triggering frequency of 2 HZ, and observe the LEDs.

Calculation:

1- Analyze the circuit of Fig.(3-1) in the two stable states.
2- Compare the function of the circuit of Fig.(3-2) with the S-R Flip-Flop.
3- Find the minimum hfe required for operation of the bistable as a function of the circuit values.

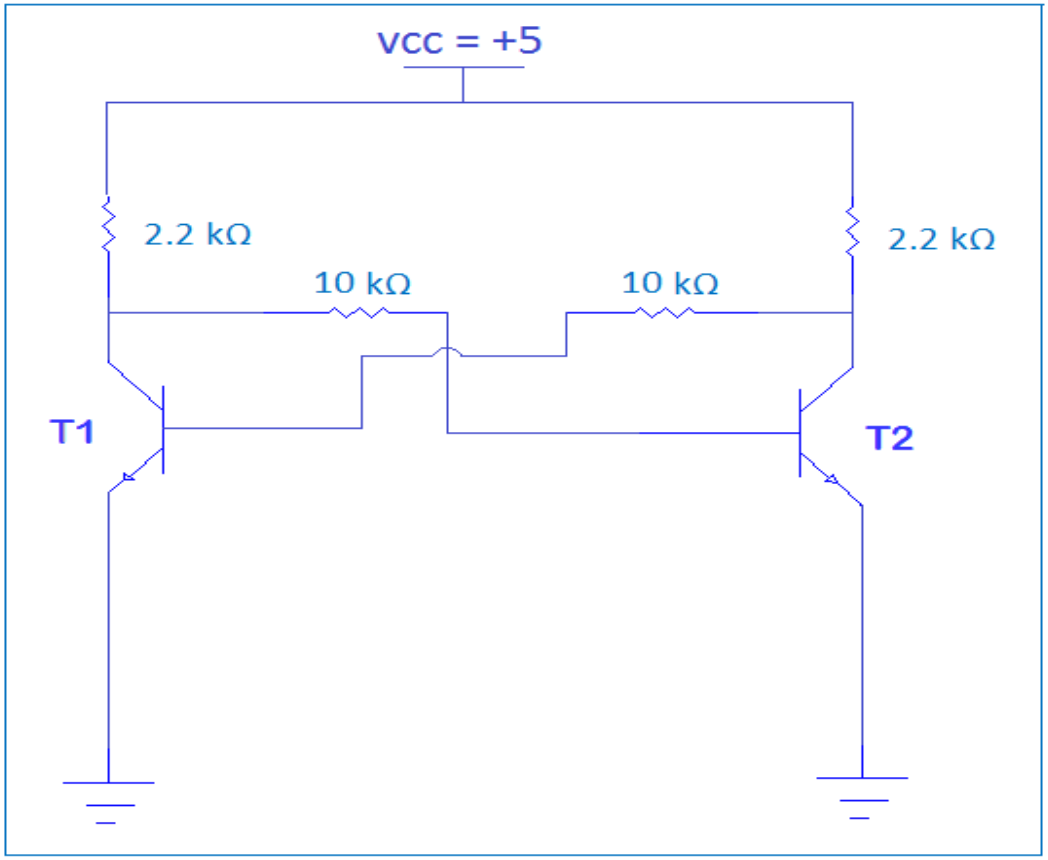


Fig (3-1)

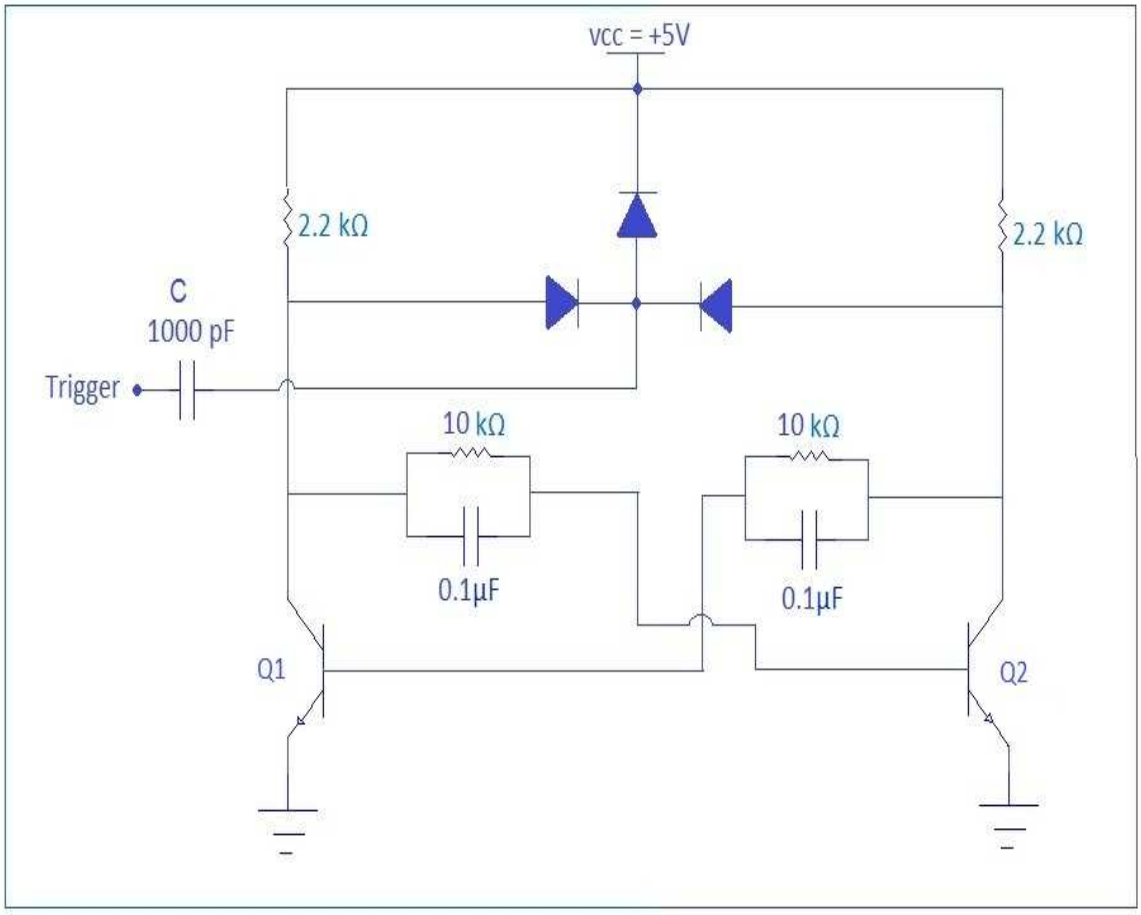


Fig (3-2)

EXPERIMENT NO. (4)
ASTABLE MULTIVIBRATOR

Objective:

To study the characteristics of the astable multivibrator and the use of the astable as a voltage to frequency converter.

Theory:

The astable multivibrator has two quasi – stable states and periodic transition occur from one state to the other. As shown in FIG (4-1) one state is with the transistor T2 non-conducting whereas the other state is the reverse of this. The output square wave contains a large number of frequencies, hence the name multivibrator. If R1 = R4, R2=R3=R and C1=C2=C, the circuit is said to be symmetrical and each transistor remains in conducting state for the same time.

In this case, the mark- to –space ratio is unity and the time period T of the oscillator is given approximately by:

T=1.4 RC seconds……(1) where R in ohms, C in farads.

F = 1/T (HZ)……..(2)

The frequency of oscillation may be varied over the range from cycles to megacycles per seconds by adjusting R or C. It is also possible to change T electrically by connecting R2 , R3 , to an auxiliary voltage according to the equation

T = 2Rc in (1+Vcc/V) ……(3)

Such a circuit is called voltage to frequency converter it is shown in Fig (4-2)

PROCEDURE:

1- Connect the circuit of FIG (4-1) and draw the wave forms of VB1, VB2, VC1, VC2 respectively with all required indications.
2- Repeat step 1 for values of R2=22K, R3=47K, C1=C2=0.1μF.
3- Connect the circuit of FIG (4-2) and change the applied voltage (V) from (1-6) volt in suitable steps (say 0.5 volt), observe the output voltage Vo and measure T corresponding to each V.

Discussion and conclusion:

Try to show the principle of operation of each circuit and discuss the outputs of the circuit and then conclude yours by comparing the theoretical and experimental results.

Questions: Derive equations 1 and 3.

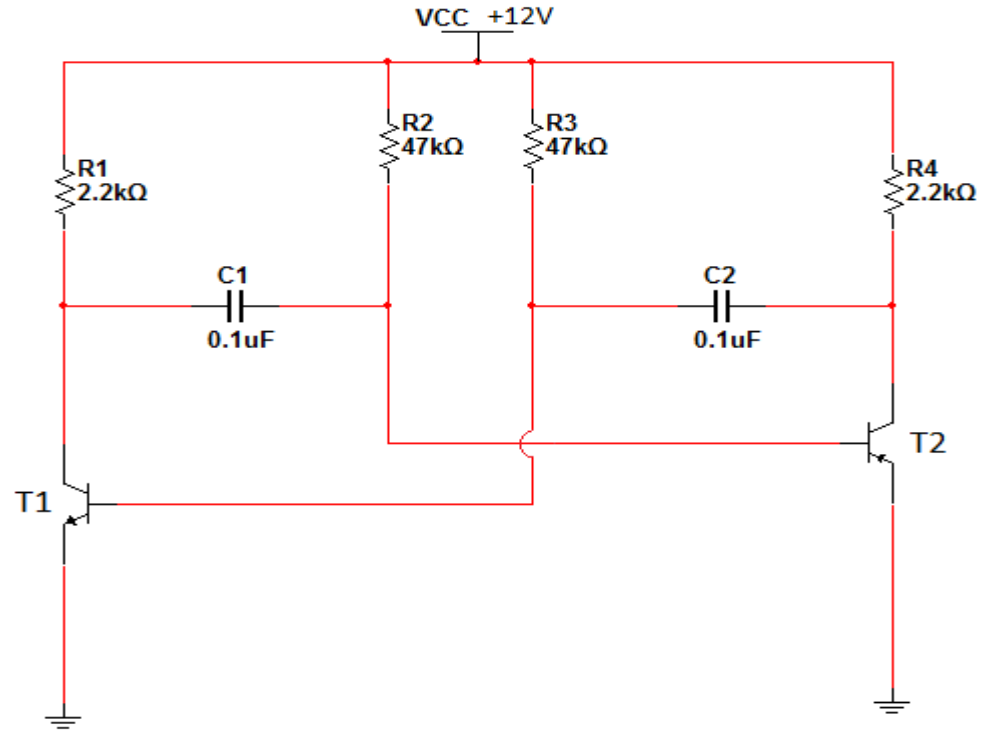

VCC +12V
R1
2.2kΩ
R2
47kΩ
R3
47kΩ
R4
2.2kΩ
C1
0.1uF
C2
0.1uF
T1
T2

Fig (4-1)

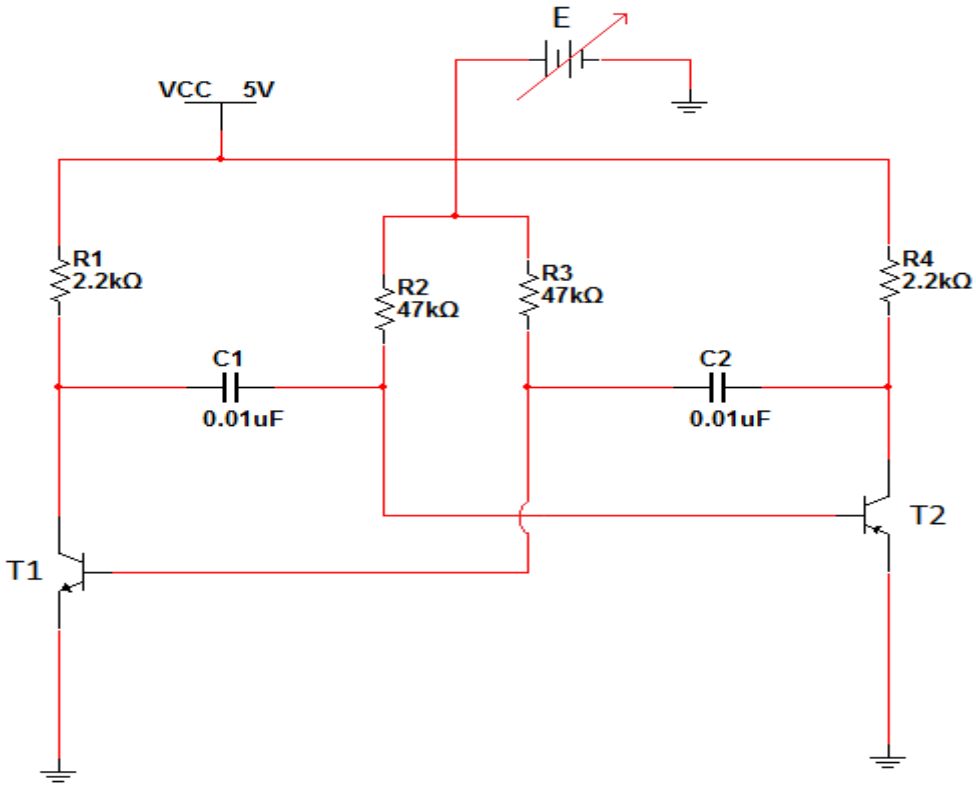

E
VCC 5V
R1
2.2kΩ
R2
47kΩ
R3
47kΩ
R4
2.2kΩ
C1
0.01uF
C2
0.01uF
T1
T2

Fig (4-2)

EXPERIMENT NO. (5)
THE MONOSTABLE MULTIVIBRATOR

Objective:

To study the monostable and to observe the internal wave forms of the monostable multivibrators, also to see the components that affects the output pulse width.

Theory:

The monostable M.V. is circuit which has one stable and one semi stable state. The circuit adopts a stable state and remains in it until an externally applied pulse (then switching signal) switches the circuit to the semi stable state. The time interval during which the circuit remains in semi-stable state is determined by the time constant of the RC circuit. At the end of this time interval the circuit returns to its sable state and remains there until a second switching signal causes it to make another transition. The trigger action of this circuit is of special importance because the switching signal can have a Varity of forms provided that its amplitude is sufficient to initiate a transition.

The output pulse waveform is always rectangular with amplitude which is independent on the amplitude or duration of the input signal.

The monostable multivibrator of fig(5-1) may be induced to make a transition out of its stable state by an application of a negative trigger at X this will drive T2 to cutoff which will make T1 to conduct because of the direct coupling from Vc2 to X , making the voltage at X to drop by (I*Rc1). The equivalent circuit of the collector of T1 is shown in FIG (5-2).

The circuit will remain in this quasi – stable state for only finite time T. point X will rie in voltage until it passes the cutoff (through the feedback coupling) returning the monostable multivibrator to its stable state .if trigger is applied at t=0, then the voltage at X will drop by I*Rc1 (i.e. VX = Vo-I*Rc1), where Vo is the V, and the time constant of the circuit will be

$T = (Rc1 + Ro)*C$

Now using the equation of the voltage rice in RC circuit which states

$V = V+ (Vo-V)\ EXP(-t/\tau)$

Where V is the final voltage, Vo is the initial voltage
We say:

$VX = Vcc – (Vcc – Vo + I*Rc1)\ EXP(-t/\tau)$ …….(1)

When VX = Vy the circuit will return to stable state and the elapsed time t=T

$Vy = Vcc-(Vcc – Vo + I*Rc1)EXP(-T/\tau)$ ……
$T= \tau \ln 2 + \tau \ln(Vcc-(Vce(sat) + V(sat))/2) / (Vcc-Vy)$
But $Vce\ (sat) + V(sat) = 2Vy$
$T= \tau \ln 2 = 0.69*(R+Ro)*C = 0.69*R*C$…….(3)

Monostable are readily and economically available in IC form and require only an external resistor and capacitor for producing the desired output pulse duration. The 74121 features positive and negative D.C level triggering inputs and complementary outputs.
When triggering occurs, internal feedback latches the cct. Prevents re triggering while the output pulse is in progress and increases immunity to negative going noise. Output pulse width stability is primarily a function of the external RX and CX chosen for the application. A 2 KΩ internal resistor is provided for optional use where output pulse – width stability requirements are less stringent. Max. Duty cycle capability ranges from 67% with a 2 KΩ resistor to 90% with 40 KΩ resistor. Duty cycles beyond this rang tend to reduce the output pulse width otherwise, output pulse width follows the relationship:

T = 0.69*RX*CX

Pin name	**Description**
A1, A`2	trigger inputs (active falling edges)
B	Schmitt trigger input (active rising edge)
Q, Q `	Outputs.

Procedure:

1- Connect the cct. of FIG (5-2).
2- Apply a pulse wave from the TTL output (0, +5V) of pulse repetition freq. (PRF) equal to 1 KHZ, and pulse duration of (100) μs.
3- Draw to scale the input and output waveforms.
4- Increase the value of R_X in 5 KΩ steps (up to 40 KΩ) and draw the output corresponding to each value.
5- Change C_X and observe the variation in t.
6- Use the internal resistor (remove RX), for CX equal to 0.01μF. And draw to scale the output waveform.

Questions:

1- Dose the shape of the triggering signal affects the cct. Operation of FIG(5-1).
2- Draw the equivalent cct. Of FIG(5-1) at the stable state and analyze it .
3- Find the max. Triggering freq. theoretically and compare it with experimental one.
4- Compare t in steps (4, 5, and 6) with the calculated value and discuss the results.

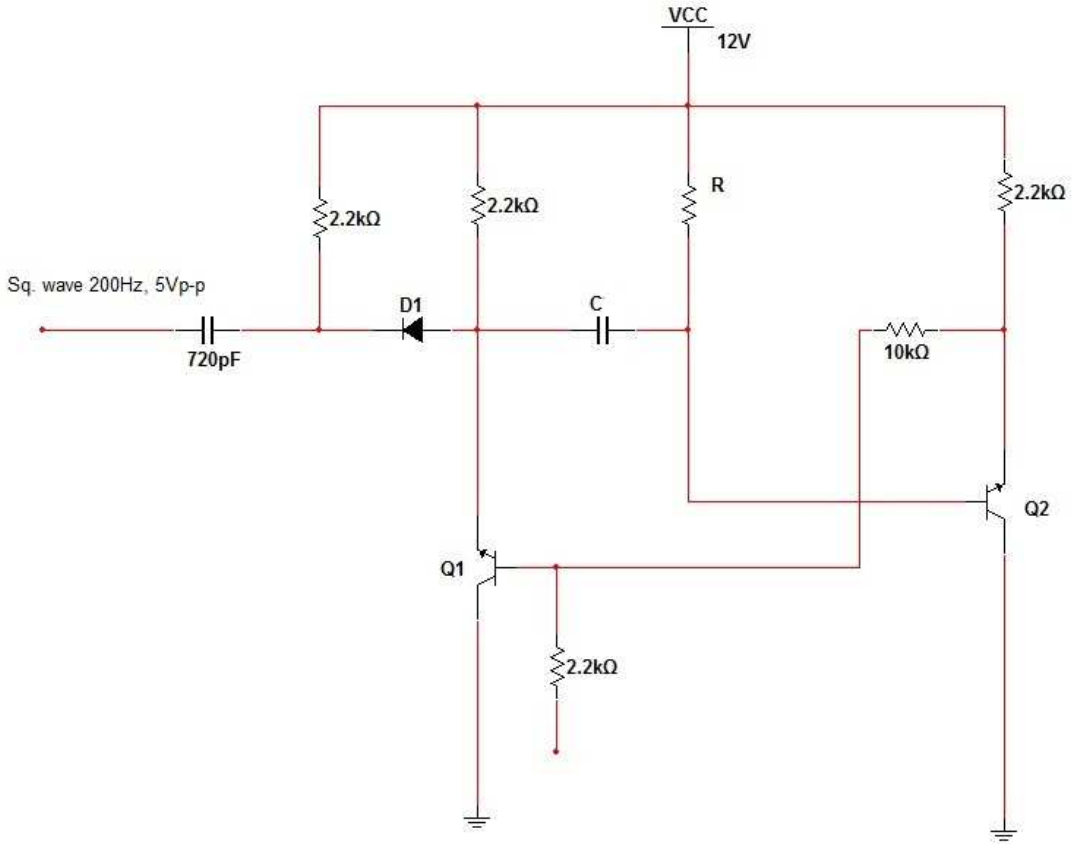

VCC
12V
2.2kΩ
2.2kΩ
R
2.2kΩ
Sq. wave 200Hz, 5Vp-p
D1
C
720pF
10kΩ
Q2
Q1
2.2kΩ

FIG (5-1)

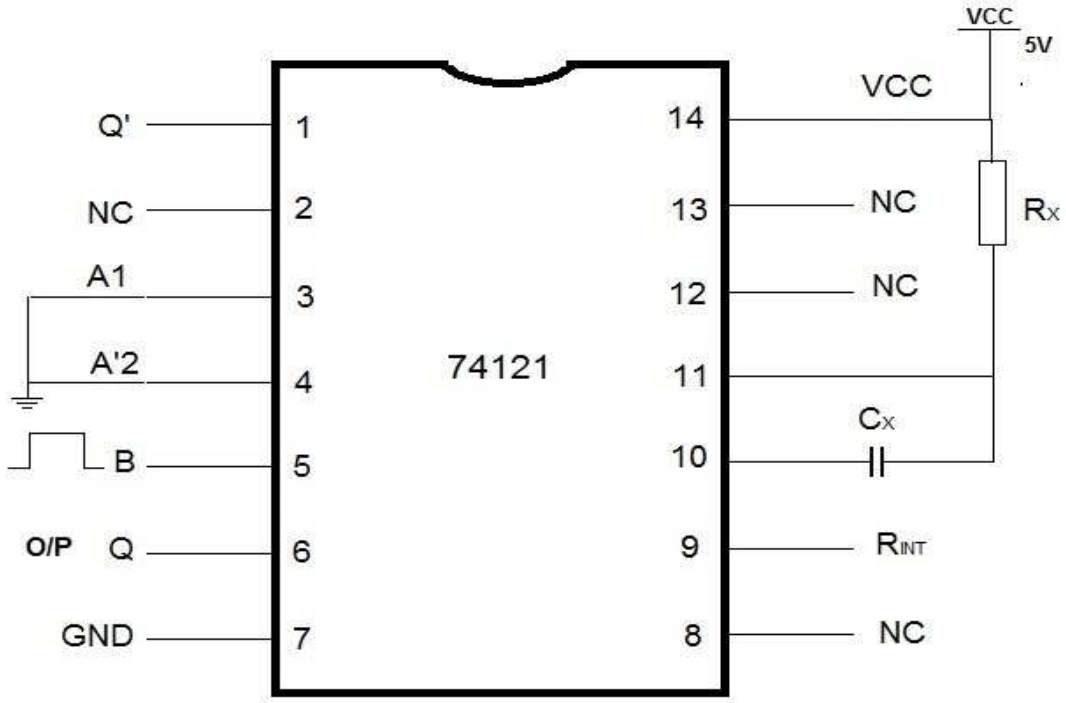

VCC
5V
VCC
Q'
1
14
NC
2
13
NC
Rx
A1
3
12
NC
A'2
4
74121
11
Cx
B
5
10
O/P
Q
6
9
RINT
GND
7
8
NC

FIG (5-2)

EXPERIMENT NO. (6)
THE SCHMITT TRIGGER

Objective:

To draw the transfer characteristic of the Schmitt trigger, and to find the circuit parameters that affects on the hysteresis of the Schmitt trigger.

Theory:

The Schmitt trigger (named after the inventor of a vacuum tube version of this circuit) is a special form of the emitter-coupled bistable multivibrator. Its stable state is determined by the amplitude of the input voltage.

In the Schmitt trigger circuit based on bipolar transistors Q1,Q2 (see fig(6-1)), when the input voltage Vi applied is zero, Q1 is at cut-off and Q2 conducts at saturation .To make Q1 conducts ,the input voltage Vi must exceed the voltage drop of the VE2 across (RE2) . The amplitude of the input voltage needed to cause Q1 to conduct is called the upper trip point (UTP). As Q1 starts to conduct, the forward bias on Q2 is reduced and a very rapid transition occurs so that Q1 conducts at saturation and Q2 is at cut-off. If now the Vi is reduced until Q1 is cut-off and Q2 conducts at saturation) the input voltage which causes this state is called lower trip point (LTP). If the input signal is sinusoidal the switching produced is shown in Fig.(6-1). The difference between (UTP) and (LTP) is called the hysteresis.

VH = UTP – LTP

To obtain a symmetrical output square wave the sine wave must be biased so that it's zero axis is in the center of the hysteresis zone.

Procedure:

1- Connect the cct. Shown in fig.(6-1) with (RB1=10K , RE2 = 1.2K)
2- Connect a D.C input voltage and vary the input D.C from (0-6)V with suitable steps and measure the output voltage for each input voltage (take more readings at the region where transition at the output voltage occur),the input voltage makes Q2 cut –off is the UTP.
3- Decrease the input D.C voltage back to zero (6-0)V with suitable steps (take more readings at the transition region), the input voltage that makes Q2 conducts at saturation is the LTP.
4- Replace RE2 with a resistor RE2=470Ω and measure UTP and LTP.
5- Apply a sinusoidal signal at (12Vp-p) and frequency of (500 HZ), then draw the output voltage. Reduce the input voltage gradually to measure the minimum amplitude required to have a square wave at the output.

Calculations & Discussion:

1- For the cct. Of the experiment find the (UTP and LTP) theoretically.
2- What do you suggest to make the output square wave symmetrical (i.e. equal times for the two parts of the cycle).

3- For the cct of the experiment it is desired to switch ON Q1 at 10 V, what resistor may be changed to provide this switching point (change only one resistor at one time) and what should be its value.
4- If the peak to peak input variation is less than the hysteresis what would be the output wave form.
5- What is the essential difference between the cct. Of Schmitt trigger and the other multivibrator circuits?

Discussion:

1- Write about the application of the Schmitt trigger.
2- Discuss the difference between the transfer characteristics obtained in step2 and step 3.

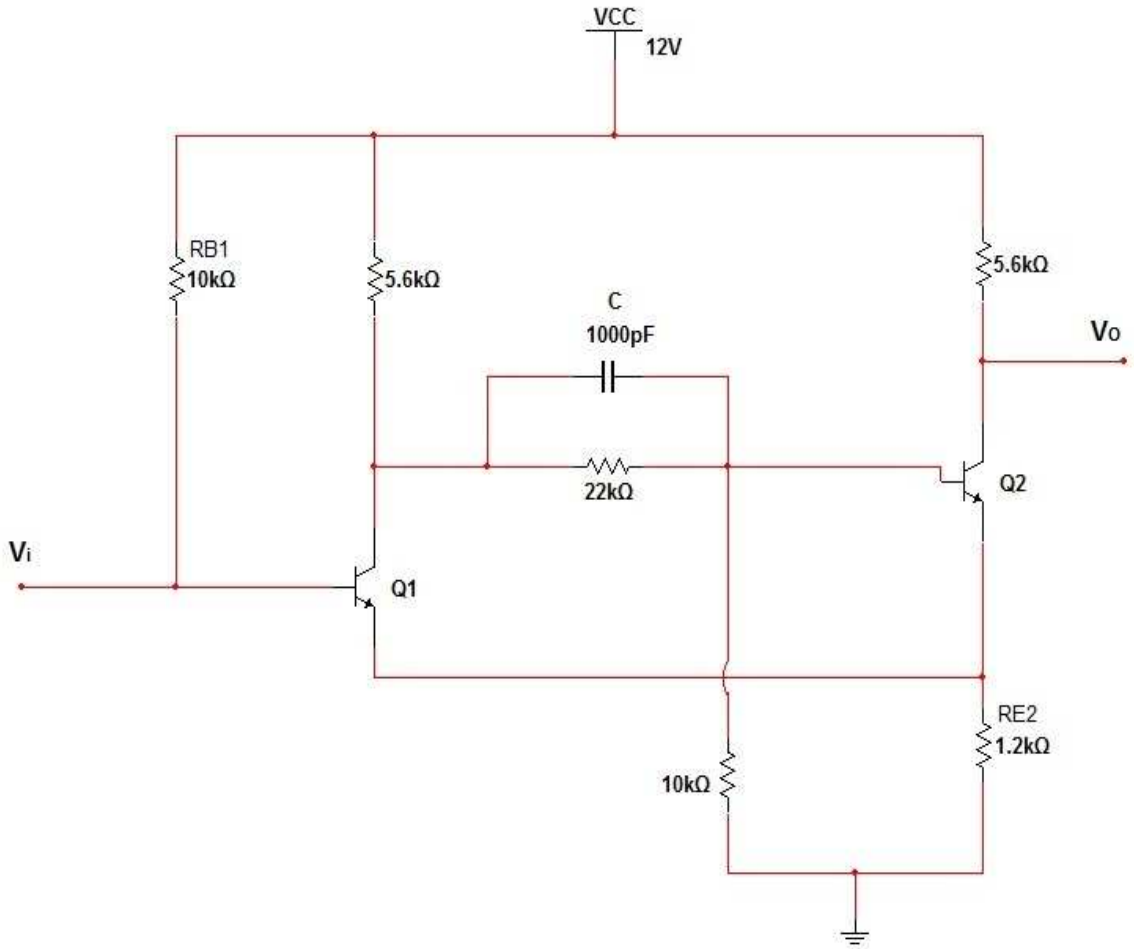


FIG (6-1) A Schmitt triggers cct. Based on bipolar transistors

EXPERIMENT NO.(7)
LINEAR INTEGRATED CIRCUIT OP.AMP.

Introduction:

A differential input op-amp is a device with two input terminals, an output terminal and two power supply terminals. In addition, it will normally have terminals for offset balancing (for setting the output to zero when the input is zero) and may have terminal to which external components can be connected in order to modify the frequency response characteristics of the amplifier. The circuit symbol for an op-amp. Is a horizontal triangle, p-amps are used with dual power supplies consisting of a positive and negative supply in series connected as shown in fig (7-1).

The two input terminals of an op-amp are normally distinguished from each other symbolically by (+) and (-) sign. Input and output signals are measured with respect to the power supply common terminal which is normally earthen.

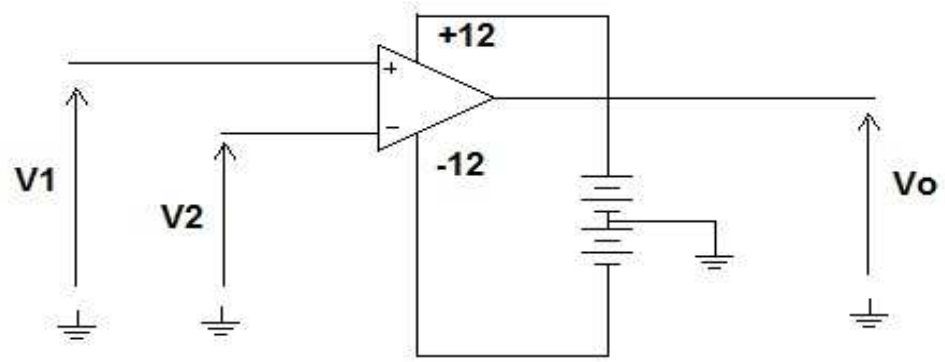


Fig (7-1) Circuit symbol used for an op-amp

1- Adder Circuit:

Vo = -(V1+V2). Verify this operation for the circuit shown in Fig (7-2) below if:

V1	+5	+5	+5	2 sin2000πt
V2	+2	-2	2 sin2000πt	2 sin2000πt

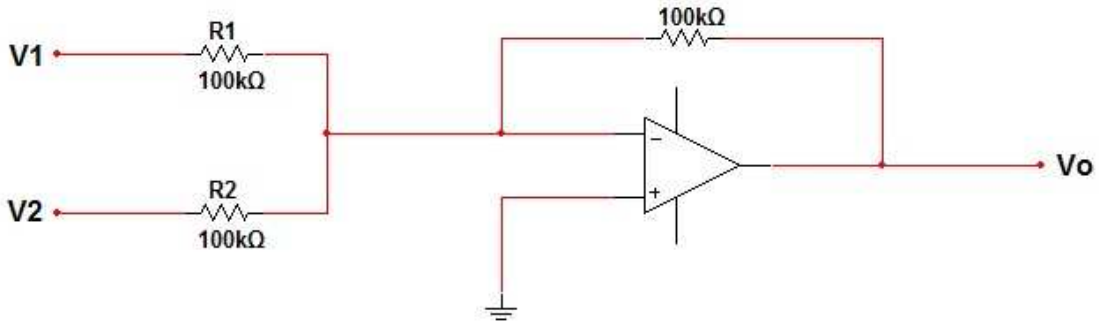


Fig (7-2) simple Adder Circuit

2- The differential amplifier :

1- Connect the circuit shown in fig(7-3)

Vo=(R2/R1)(V2-V1).

V1(v)	-5	-4.5	-2	2	2
V2(v)	+4.5	+5	-3	1.5	3

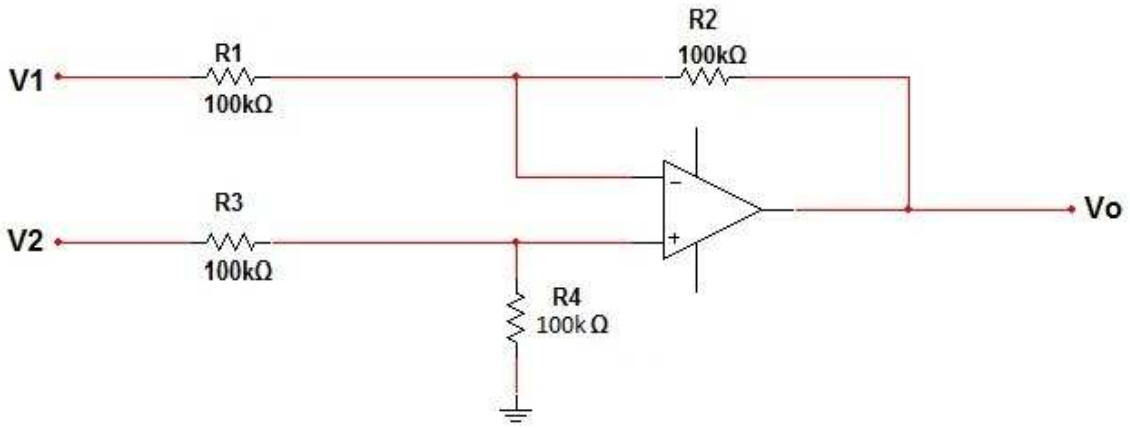


Fig (7-3) Simple Differential Amplifier

3- Measurement of output resistance Ro

For the circuit shown in fig (7-4):

a- Measure Vo.

b- Connect a variable load resistance to the output cct. And record the value o RL for: Vo=1/2 VOL, Ro=RL

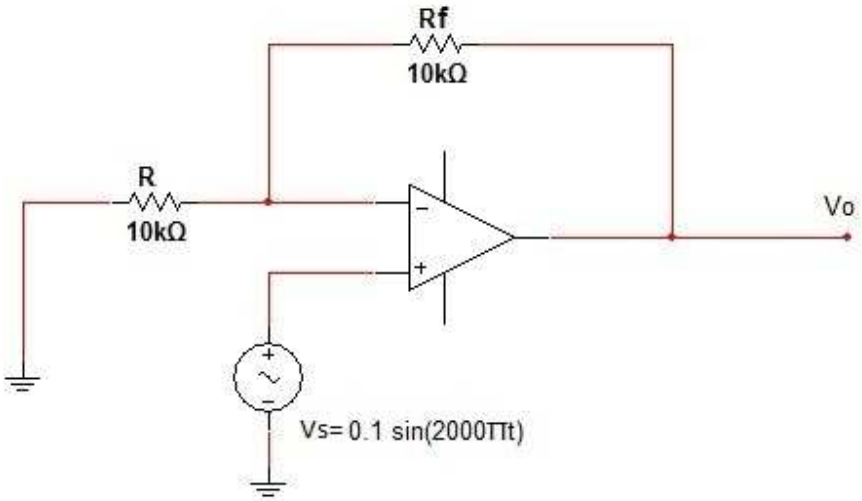


Fig (7-4)

4- C.M.R.R (ρ) Measurement:

a- Connect the cct. as shown in fig (7-5) if :

R=R1=100Ω

Rf=R`1 =100KΩ

Vs= 0.1 sin (2000πt) V

b- Find the value of (ρ) if:

P=(Ad)/(Ac) = ((Vo)/(Vi)) / ((Vo)/(Vc)) =(Vc) / (Vi) = (Vs) / (Vi)

(Vo)/(Vi)=(R+Rf)/(R)

(ρ) = ((R+Rf)/R)*((Vs)/Vo))

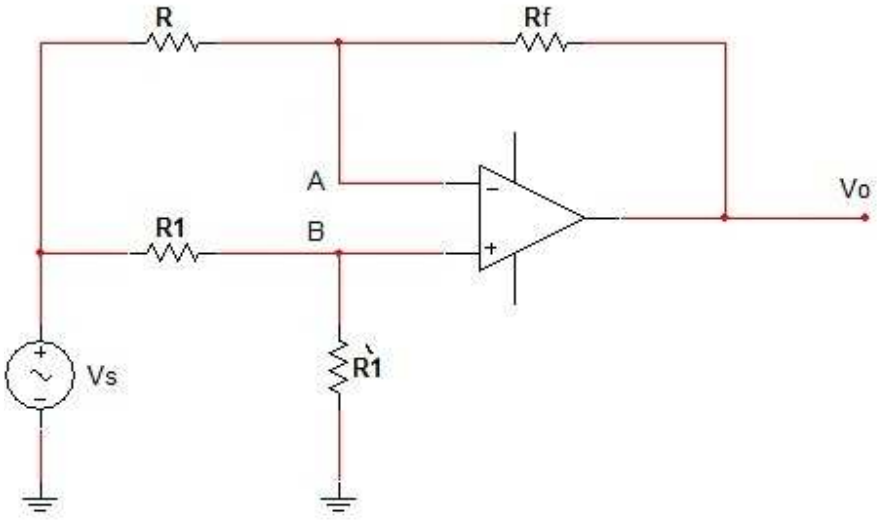


Fig (7-5)

5- sine – wave Generator:

a- Connect the cct. As shown in fig (7-6).

b- Draw the output waveform.

c- Derive the two conditions of oscillation:
(VA = VB =1/3), (Fo = 1/2πRC)

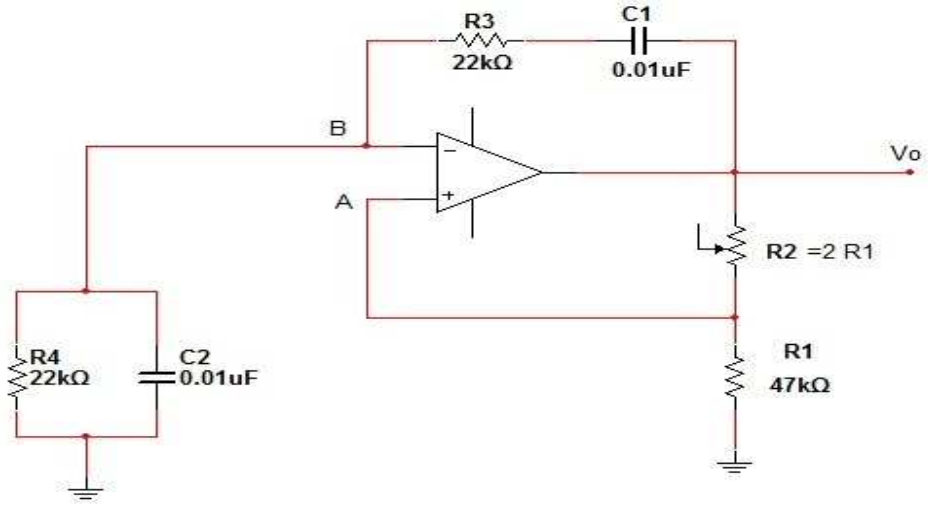


Fig (7-6) Sine wave generator

6- Square-Wave Generator:

a- Connect the cct. as shown in fig (7-7).

b- Draw VA, VB, Vo.

c- Measure T for the values shown in the table below:

C(μF)	R2(KΩ)	R3(KΩ)
0.01	100	220
0.01	470	220
0.01	20	220

d- Derive the equation of (T)where:
T= 1/F=2*Rf *ln((1+β)/(1-β))

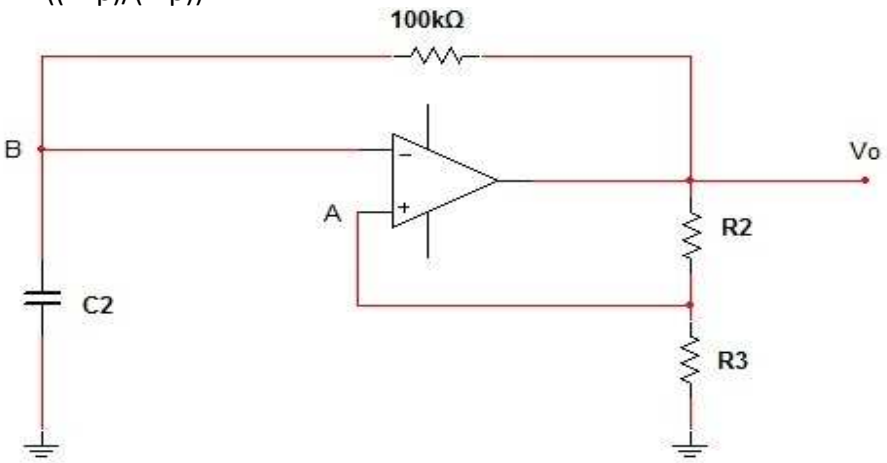


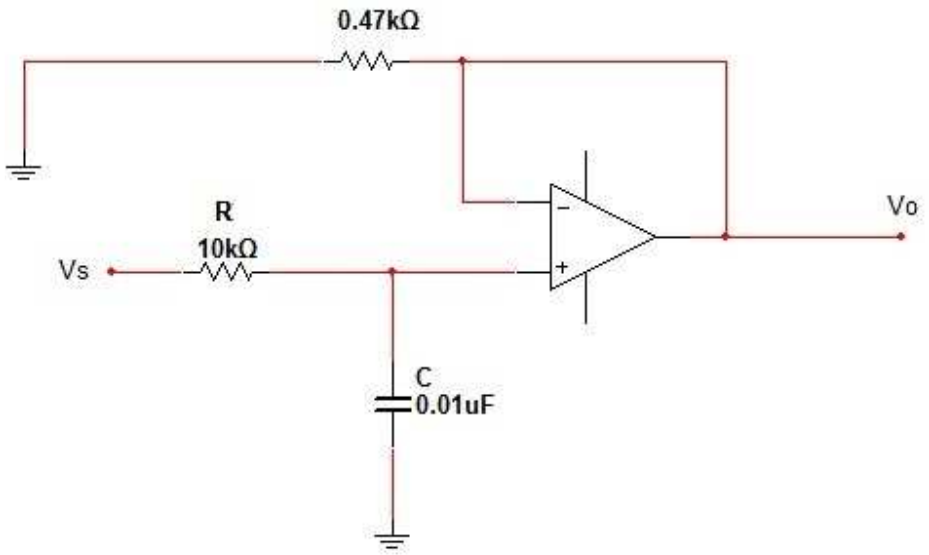
Fig. (7-7) square wave generator

7- Low-Pass Filter (L.P.F):

a- Connect the cct .as shown in fig (7-8).

b- Change the frequency from (50-20K)Hz and measure Vo.

c- Draw the frequency response curve then find the cut-off frequency, Where:
Fc = 1/2πRC.



Vs = sin (2πft)

Fig (7-8) LPF

8- High-Pass Filter (H.P.F.):

Repeat steps (1-3) of L.P.F circuit for the cct. Shown in fig (7-9).

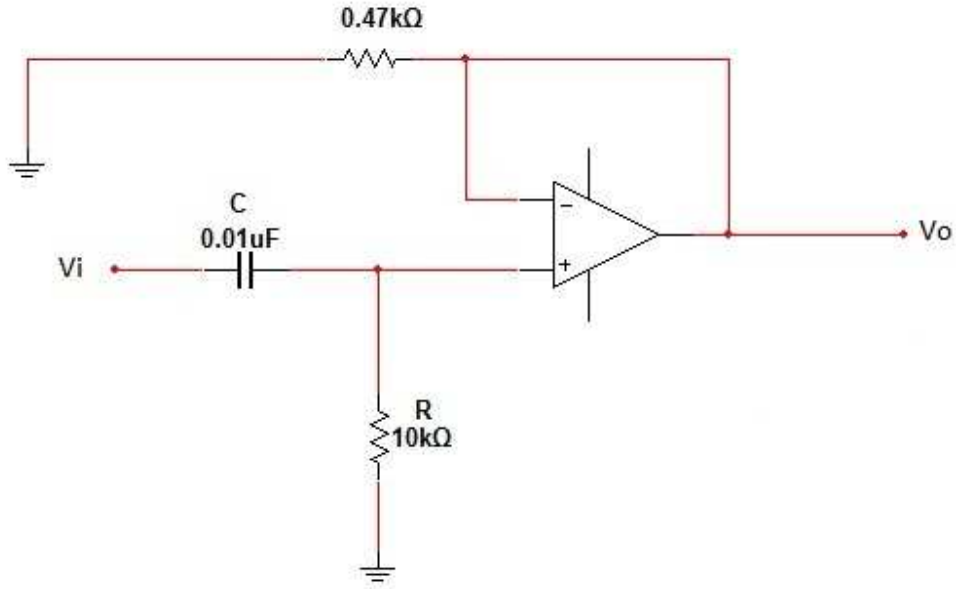


Fig (7-9) HPF

9- Determination of Input impedance:

1-while the power supply off, construct the cct. Show in Fig (7-10).
2-Turn on the power supply, and set the sine- wave generator to (1000) Hz.
3-Adjust the generator output amplitude for maximum undistorted signal at Vout.
4-Record the peak- to- peak value of Vin.
5-Place the oscilloscope Probe to position B .Adjust Rp until the peak- to- peak value of Vin is one- half the value recorded in step 4.
6-Record the value of Rp .This resistance value is equal to input impedance of the op- amp.
7-Repeat step 2 through 6 for the following frequencies:
100Hz, 10Hz, and 100 KHz.

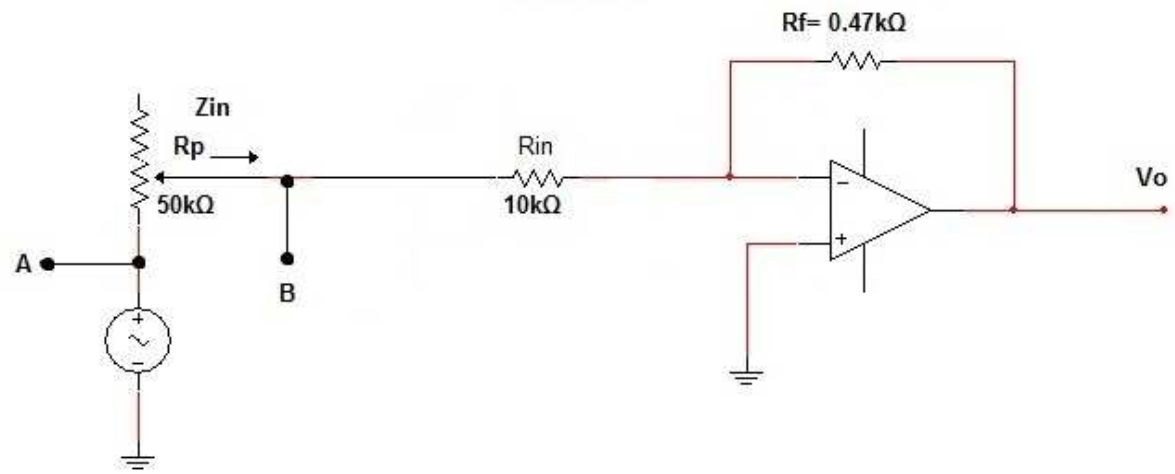


Fig (7-10) input impedance

Discussion:

1- What is the input impedance of op-amp?
2- Does the input impedance change with different input signal frequencies?

EXPERIMENT NO. (8)
HALF AND FULL ADDERS

Introduction:

Digital computers perform a variety of information- processing tasks. Among the basic functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition of two binary digits. This simple addition consists of four possible elementary operations namely, 0 + 0 =0,0+1=1, 1+0=1, 1+1=10. The first three operations produce a sum whose length is one digit, but when both augends and addend bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a carry. When the augends and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next
Higher-order pair of significant bits. A combinational circuit that performs the addition of two bits is called a(half-adder).One that performs the addition of three bits(tow significant bits and a previous carry)is a(full-adder).The name of the former stems from the fact that tow half-adder can be employed to implement a full-adder.

HALF-ADDER: From the verbal explanation of a half-adder, we find that this circuit needs tow binary inputs and tow binary outputs:

B	A	carry	Sum
0	0	0	0
0	1	0	1
0	0	0	1
1	1	1	0

The carry output is 0 unless both inputs are 1.The sum output represent the least significant bit of the result.
The Boolean functions for the tow outputs:
Sum=A$\oplus$B ……(1)
Carry=A.B ……(2)
Fig (8-1) represent the implementation of the half-adder.
Full – Adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. The third input, Ci, represents the carry from the previous lower significant position. The truth table of the full – adder is as follows:

A	B	Ci	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The full –adder can be implemented with two half – adders and OR gate. The sum output from the second half-adder is the EX-OR of Ci and the output of the first half – adder, giving:

Sum = Ci $\oplus$ (A $\oplus$ B)

=AB`C`i +A`BC`i +ABCi +A`B`Ci……..(3)

Carry =AB +ACi +BCi……(4)

Procedure:

1- Connect the circuit of Fig.(8-1)A. Verify its truth-table.
2- Connect the circuit of Fig.(8-2)B. Verify its truth – table.

DISCUSSION:

1- Draw the full- adder circuit using NAND gates only.
2- Derive equation (4).
3- Construct a full- adder using half- adder circuit.
4- Construct a binary adder that adds two 5 – bit numbers.

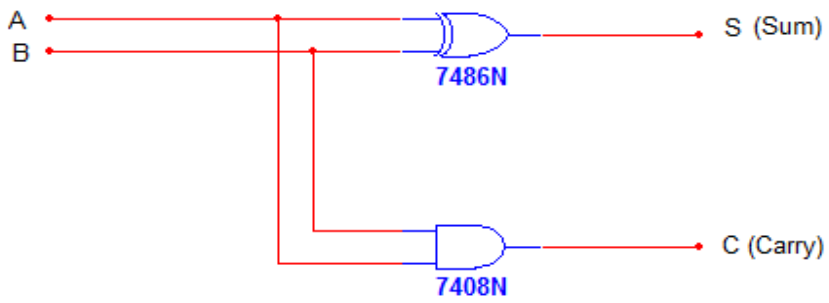


Fig. (8-1)A
Half Adder Circuit diagram

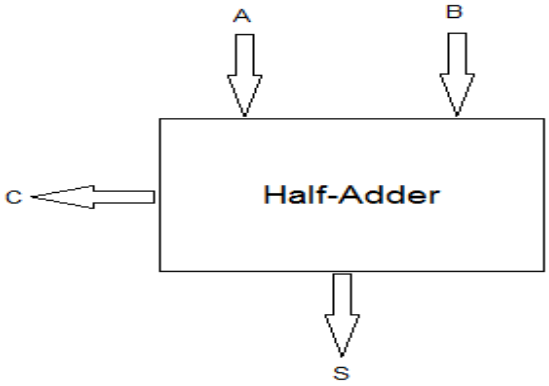


Fig. (8-1)B
Half Adder block diagram

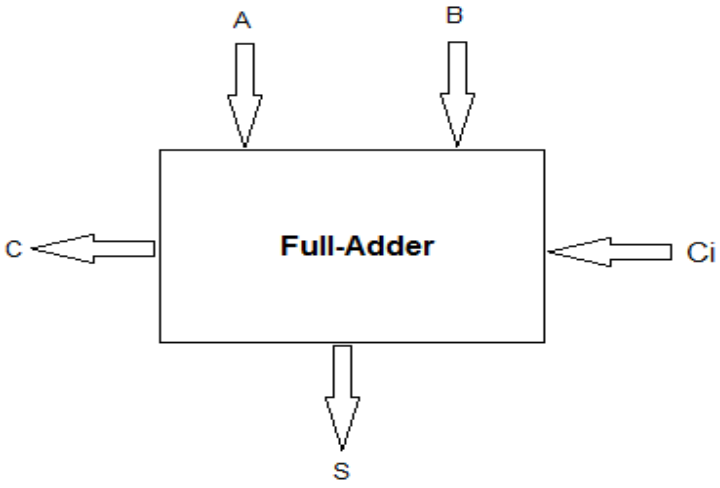


Fig. (8-2)A
Full-Adder block diagram

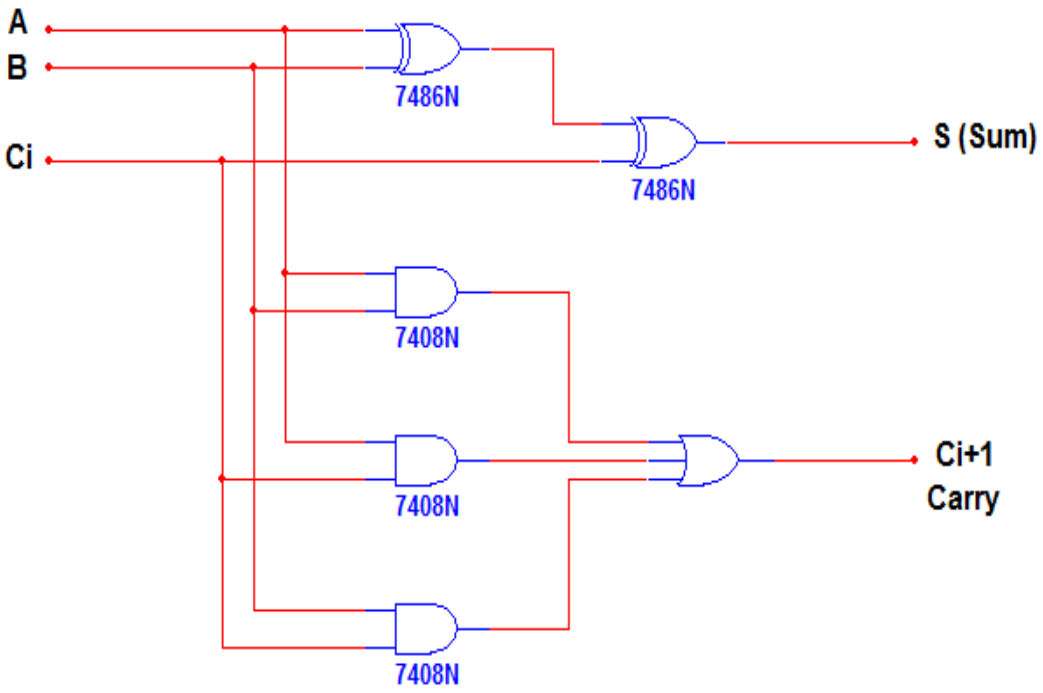


Fig. (8-2)B
Half-Adder circuit diagram

EXPIERIMENT NO. (9)
MAGINITUDE COMPARATOR

Objective:

Design and implementation of magnitude comparator circuit by using the IC (7485).

Introduction:

The comparison of two numbers is an operation that determines if one number is greater than, less than, or equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicates whether A >B, A = B or A<B.

The operation of a two one bit comparator can be described by following truth-table:

A	B	E (A = B)	G (A > B)	L (A < B)
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

According to the truth table, the Boolean equation will be as follows:

E = A` B `+AB …….. (1)

G = A B ` …….. (2)

L = A` B …….. (3)

Equation (1) represents a (2 – input) EX – NOR gate, and can be rewritten as:

E = A $\odot$ B = $A \oplus B$ = A B + A B …….. (4)

Therefore, from equation, (4),(2),(3),a 1 – bit magnitude comparator logic circuit can be implemented as shown in Fig (9-1).

Note: MSI IC 7485 is a 4-bit magnitude comparator.

Procedure:

1- Connect the circuit shown in fig.(9-1)
2- Construct the truth – table.
3- Connect the circuit shown in fig. (9-2).
4- Construct the truth – table.

Discussion:

1- Design a 1 –bit magnitude comparator using (NAND) gate only.
2- Design a 3- bit magnitude comparator using (NAND) gates only.
3- Design a 3- bit magnitude comparator using the 7485 IC. Write down its truth – table
4- Design an 8 – bit magnitude comparator, using the 7485 ICS.

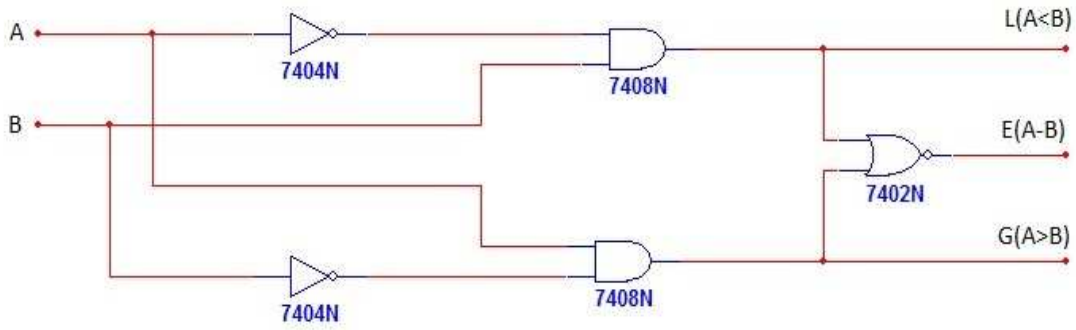

A
B
7404N
7404N
7408N
7408N
7402N
L(A<B)
E(A-B)
G(A>B)

Fig (9-1)

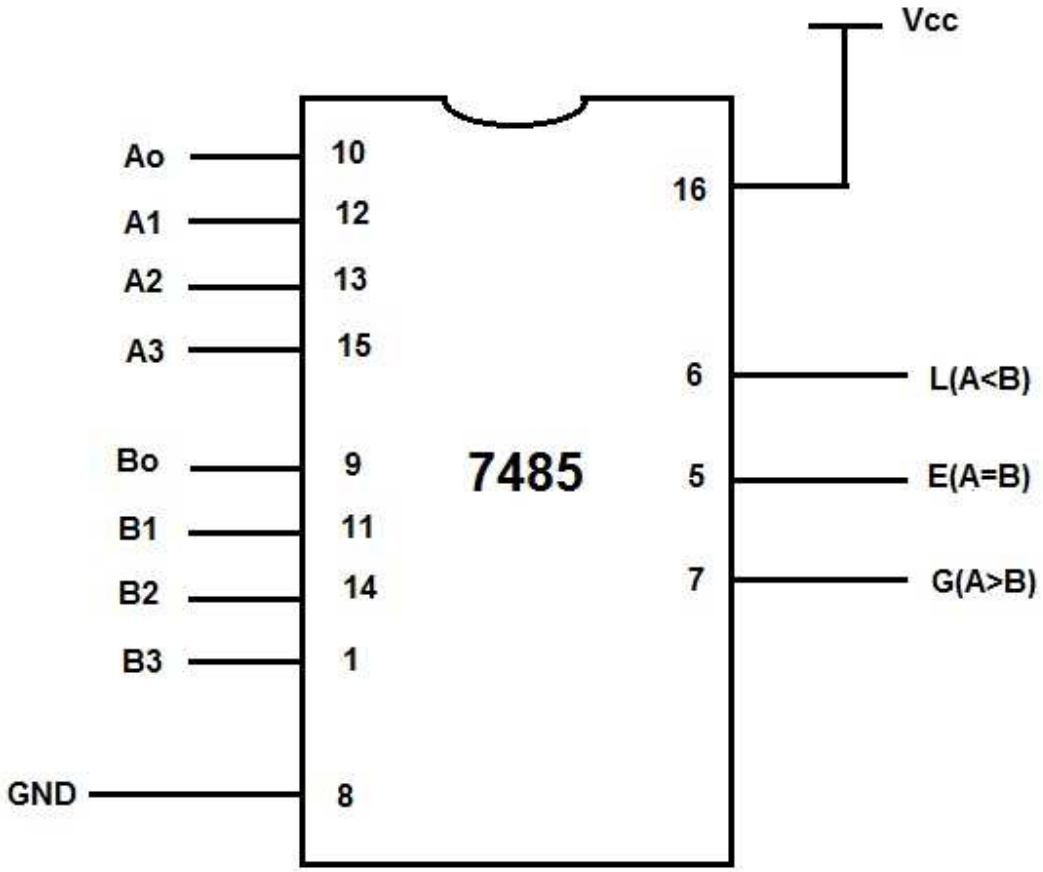

Vcc
Ao
A1
A2
A3
Bo
B1
B2
B3
GND
10
12
13
15
9
11
14
1
8
16
6
5
7
7485
L(A<B)
E(A=B)
G(A>B)

Fig (9-2)

EXPERIMENT NO. (10)
PARITY CHEKER AND CONTROLLED INVERTERS

Objective:

To introduce some important applications of the XOR logic gate, such as parity checker / generator and controlled inverters.

Introduction:

a- Parity checker/ generator: A parity bit is scheme for detecting errors during transmission of binary information. A parity bit is an extra bit included with the binary massage to make the number of 1s either odd or even .The massage including, the parity bit, is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond to the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator ,the circuit that checks the parity in the receiver is called a parity checker

The parity of a binary word can be determined with an XOR gate circuit.

b- Controlled inverter: Another application of XOR gate is the controlled or programmed inverter. See fig. (10-2)

When the input, control, is low, it transmits the binary word to the output (unchanged). But when, control, is high it transmits the 1s complement.

Procedure:

1- Connect the circuit shown in Fig (10-1).
2- Derive the truth – table.
3- Connect the circuit shown in Fig (10-2). Repeat step (2).
4- Connect the circuit shown in Fig (10-3).Repeat step (2).

Discussion:

1- Write down the Boolean equation for Fig(10-3)
2- Construct a truth –tale and add to the binary code, the odd- parity bit. Draw the logic circuit using NOR gates.
3- How many NOR gate do we need to construct a controlled inverter for 48 – bit word.
4- Repeat step (3) for NAND gate.

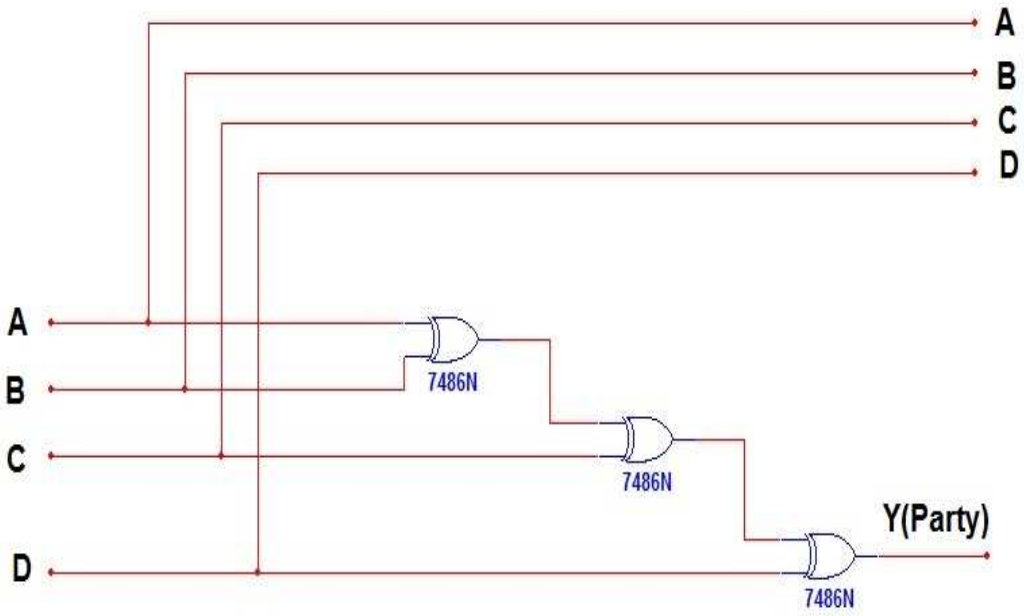


Fig (10-1) Party Checker

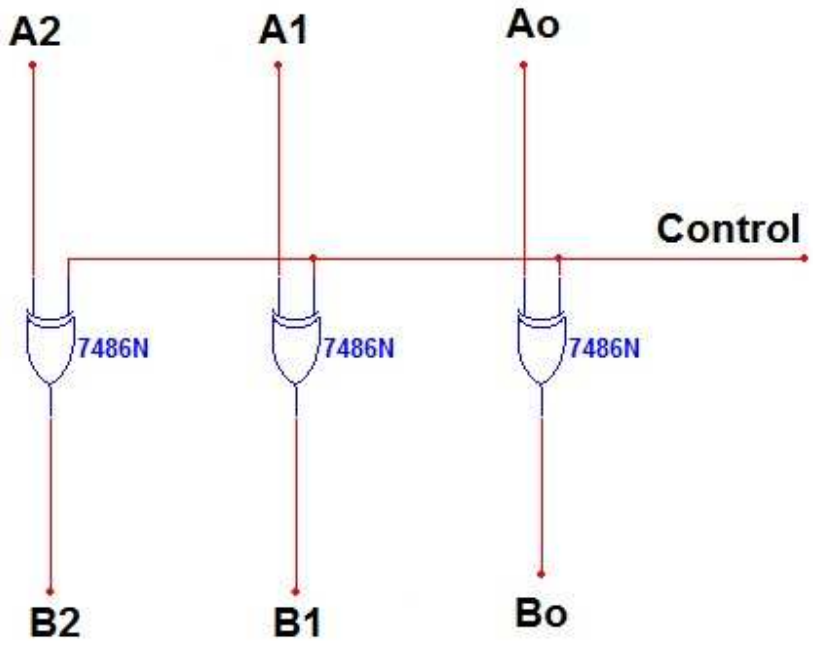


Fig (10-2) Controlled Inverter

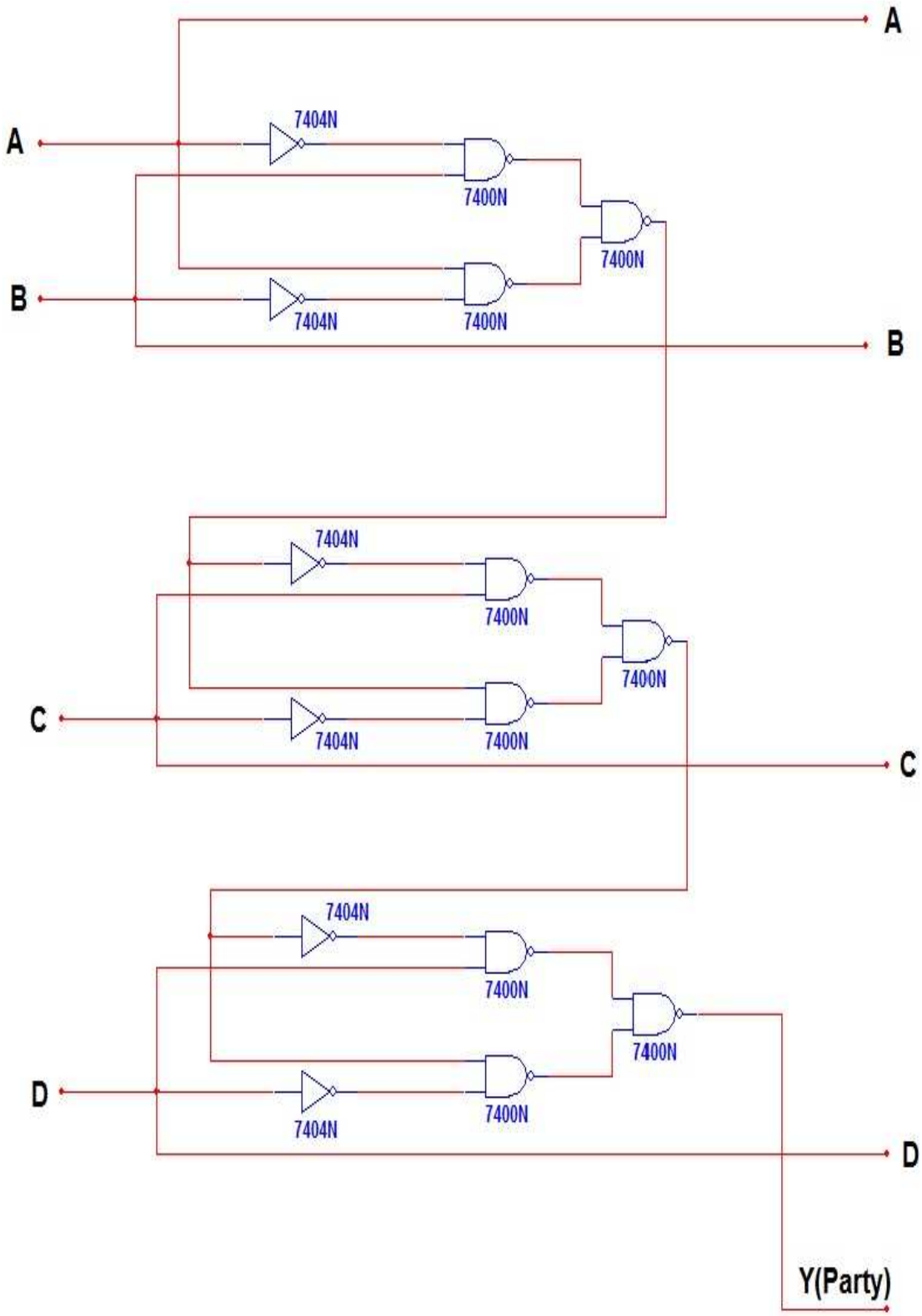


Fig (9-2) Party Checker

EXPERIMENT NO. (11)
BINARY – TO – GRAY GRAY – TO – BINARY
CODE CONVERSION

Objective:

To be familiar with the "GRAY – CODE "and the conversion from binary – to – gray and vice – versa. Also, to implement binary – to – gray and gray – to –binary code conversion.

Theory:

The gray code is an unweighted code not suited to arithmetic operation, but useful for input – output device, analog – to – digital converters, shaft encoder , and other peripheral equipment.

Table (1) shows the gray code, along with the corresponding binary numbers. The feature of Gray code is that in progressing from one number to the next in sequence one only of the binary digits (bits) suffers a change.

	BINARY			-	GRAY			
DICIMAL	A	B	C	D	X1	X2	X3	X4
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1.	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

Table (1)

Sometimes, we have to convert binary numbers into Gray code numbers and vice versa. A Binary- Gray code converter is a device for converting a binary number applied at its input terminals into the equivalent Gray code number at its output terminals as shown in fig.(11-1).

For instance, in converting from Binary digit (A) .Add each pair of adjacent bits to get next Gray digit as follows:

X2 = A+B, X3 = B+C and X4 = C+D

And to convert from Gray code to binary we use the following formula:

A =X1 B=A+X2

C=B+X3 and D=C+X4

Fig. (11-2and 11-3) shows a way to build a 4-bits binary-to-Gray and gray-binary converter by using exclusive – OR circuits.

Procedure:

1- Connect the cct. As shown in fig.(11-2).
2- Use all combinations of states of switches (A, B, C, and D) to get the data of table (1). Note that the lamps (X1, X2, X3, and X4) display the gray code number.
3- Re – arrange the cct. Connected in step (1) to be as shown in fig.(11-3). The cct. In this case will be a Gray- to – binary converter instead of binary – to – Gray converter.
4- Use all combinations of states of switches (X1, X2, X3, and X4) to get the data of table (1), and note that lamps (A, B, C and D) display the binary number.

Discussion:

1- Convert the following Gray numbers into binary number :

a- 10101 b-100110011 c- 00111000100110

2- Convert the following binary numbers into Gray number :

a- 1010110 b-1011001001 c- 10101101110011

3- Draw a logic circuit that converts 10-bits binary numbers into Gray code numbers, use exclusive – OR gates.
4- Draw a logic circuit that converts 10 – bits Gray numbers into binary numbers, use exclusive – OR gates.

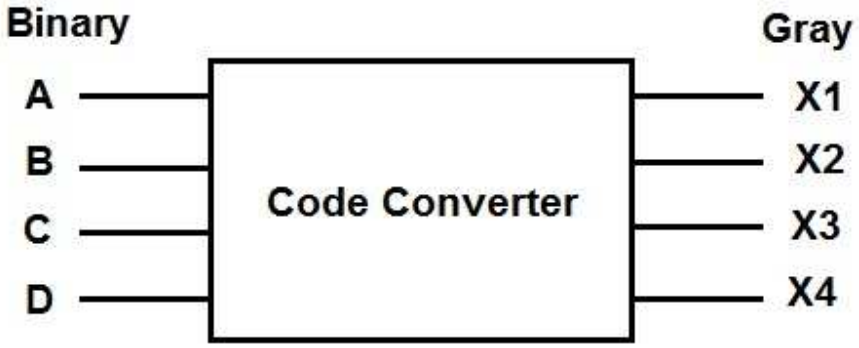


Fig (11-1)

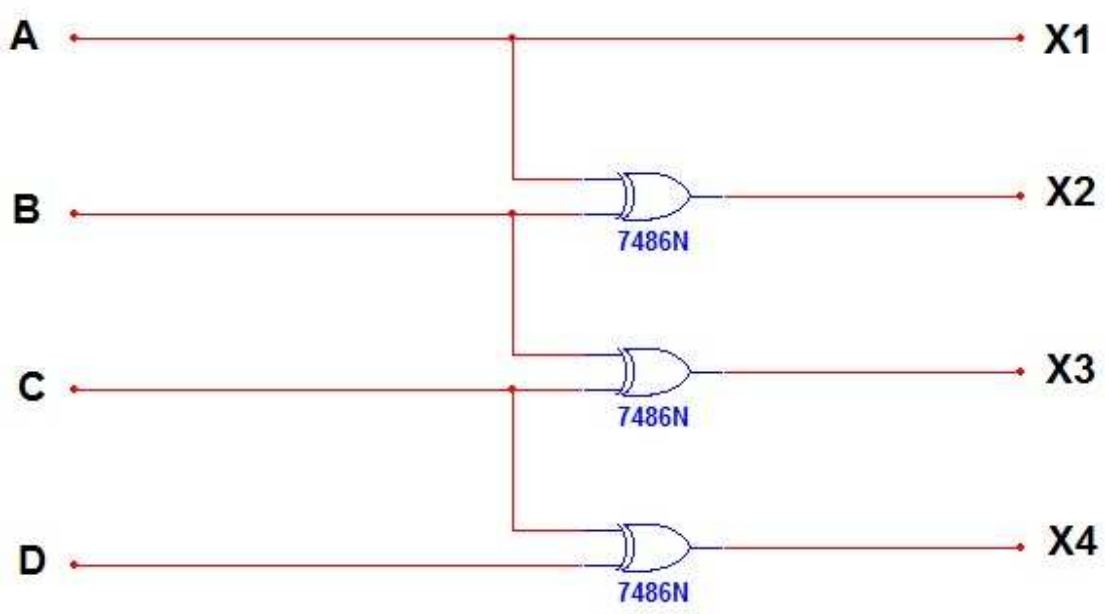


Fig (11-2) Binary-to-Gray Convertor

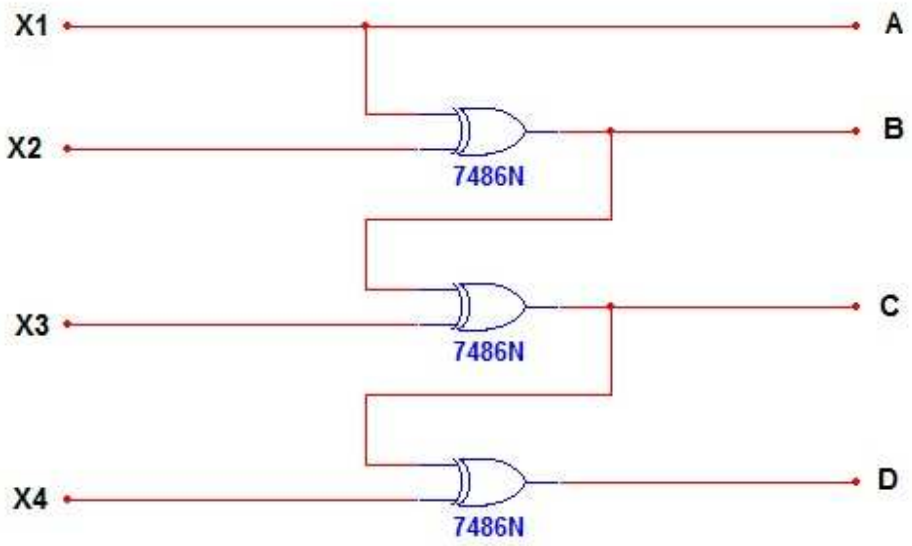


Fig (11-3) Gray - to – Binary Converter

EXPEREMENT NO.(12)
2 S COMPLEMENT ADDER-SUBTRACTOR

Objective:

in this experiment you will construct and test adders and subtractors, by using the IC type (7483) which is a 4-bit binary parallel adder.

Introduction:

The IC 7483 consists of four full – adder stages used to add two four – bit number, as in fig (12-1). The pin assignment is shown in Fig (12-1).The pin assignment is shown in Fig (12-2). The two 4-bit input binary numbers are A1 through A4 and B1 through B4. The 4-bit sum is obtained from S1 through S4. (Ci) is the input carry and (Co) is the output carry.

The subtraction of two binary numbers can be done by taking the 2 s-complement of the subtrahend and adding it minuend. The 2 s complement can be obtained by taking the 1 s complement and adding 1. To perform A – B, we complement the four bits of B, add them to the four bits of A, and add 1 through the input carry. This is done in Fig (12-3). The four XOR gates complement the bit of B when the mode M = 1 (because X $\oplus$ 1=X↓) and leave the bits of B unchanged when M = 0 (because X $\oplus$ 0 = X). Thus, when the mode M equal to, 1, the input carry Ci equal to, 1, and the sum output is A plus 2's complement of B. When M is equal to 0, the input carry is equal to 0 and the sum generates A+B.

Procedure:

1- Connect the adder – sub tractor circuit of (12-2) and test it for proper operation.
2- Connect the circuit of Fig (12-3) connect the four A inputs to a fixed binary number (1001) and the B inputs to switches.
3- Perform the following operation and record the values of the output sum and the carry output (Co).

9+5	9-5
9+9	9-9
9+15	9-15

Discussion:

1- Discuss the values of the output when: the sum exceeds 15; A≥ B; and when A<B.
2- Design a 1's complement subtractor using the IC 7483.
3- Design an 8- bit binary adder using the 7483 IC's.
4- Show, how the adder-subtractor circuit can be used as a magnitude- comparator.

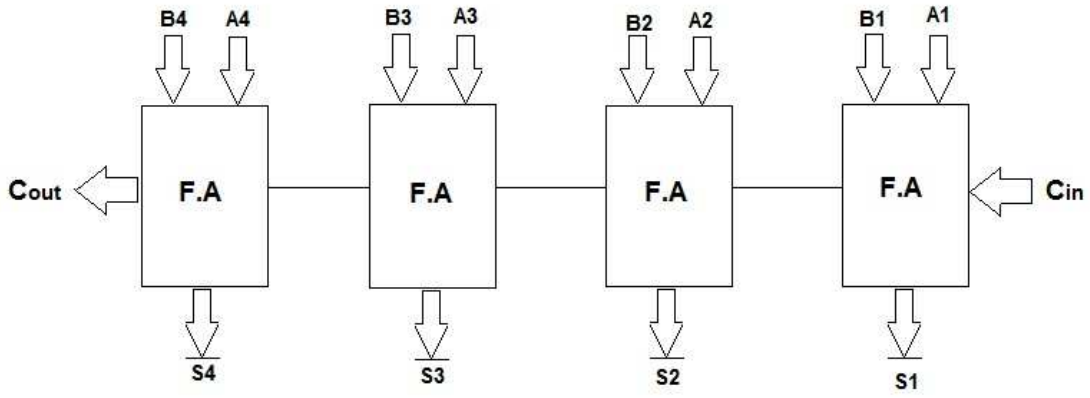


Fig (12-1)

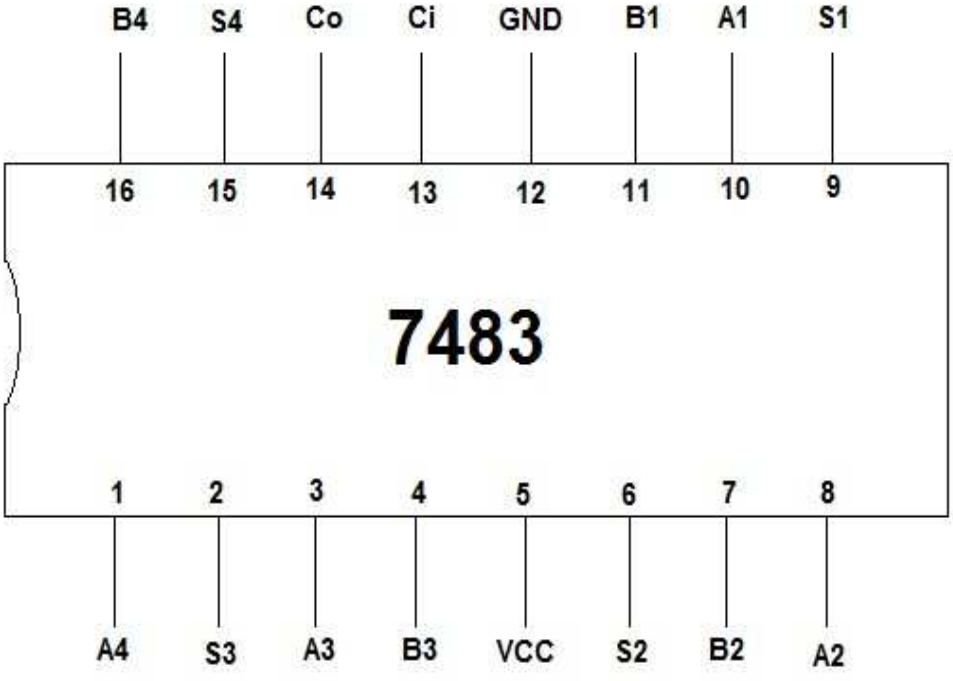


Fig (12-2)

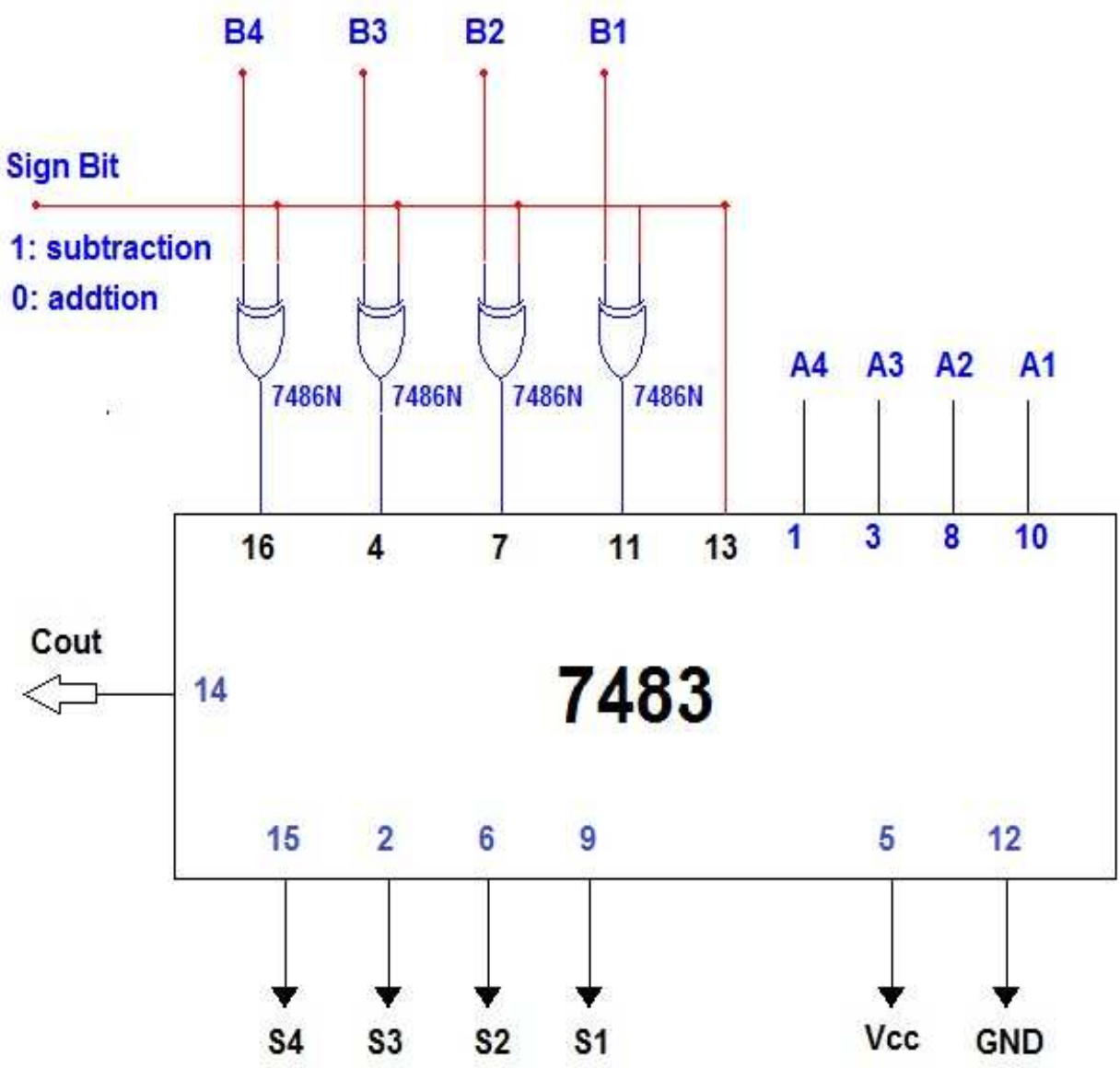


Fig (12-3) Adder-Subtractor Circuit

EXPEREMENT NO. (13)
FLIP-FLOPS

Introduction:

Flip - flops are binary cells capable of storing one bit of information. A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states. The major differences among various types of flip-flops are in the number of inputs they possess and in the manner in which the inputs affect the binary state. The most common types of flip-flops are discussed below.

SR –flip– flop:

This flip-flop circuit can be construct from two NAND gates as shown in Fig. (13-1). The cross- coupled connection from the output of one gate to the input of the other gate constitutes a feedback path. For this reason, the circuit is classified as asynchronous sequential circuit.

- Connect the circuit of Fig. (13-1) verify experimentally its truth – table.

Clocked SR flip-flop:

By adding gates to the inputs of the SR-F.F, the flip-flop can be made to respond to input levels during the occurrence of a clock pulse, see Fig. (13-2).

- Connect the clocked –SR-F.F circuit (use the manually synchronizing pulses to operate the circuit)
- Notice, that the output of the circuit will be affected only when a clock pulse comes.

MASTER / SLAVE JK:

AJK flip-flop is a refinement of the RS flip-flop in that the indeterminate state of the RS type is defined in the JK type.

1- Connect the IC in Fig. (13-3). Tie J1, J2, J3 together also K1, K2, and K3 must be tied together.
2- Verify the truth- table, using the manual synchronizing pulses from the pulse generator.

M/ S JK flip– flop to T flip-flop conversion:

1- Tie the inputs J and K together to form the T input. See the figure.
2- Operate the circuit using suitable frequency.
3- Draw the waveform of Q when T = 1
4- Verify, experimentally the truth- table:

T	Q n+1
0	Qn
1	Qn

M/ S JK flip– flop to D flip-flop conversion:

1- Connect the circuit shown in the figure. (J = D = K).
2- Verify, experimentally , the truth – table :

D	Qn+1
0	0
1	1

Report:

1- Draw the circuit of SR-F.F. by using NOR gates. Write down the truth-table.
2- Draw the complete logic circuit of the M / S flip-flop.
3- What are the meanings of the following abbreviations, T, R, and S.?
4- What is the importance of T – Flip-flop and D flip-flop?
5- What is the advantage of M/S configuration, of flip-flops?

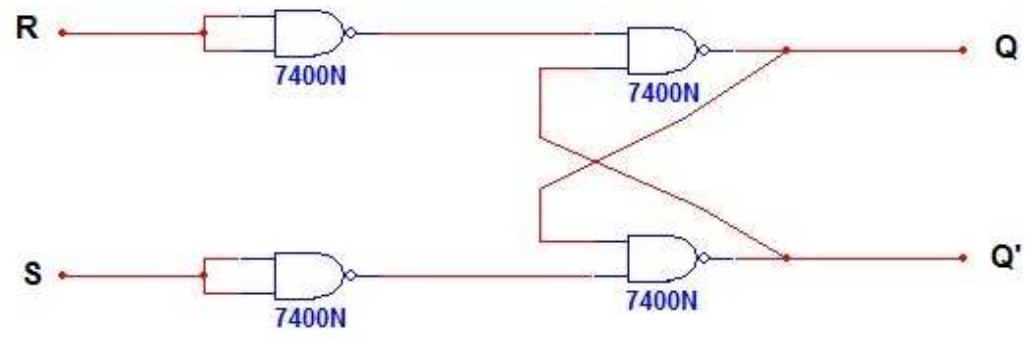


Fig (13-1) RS flip-flop

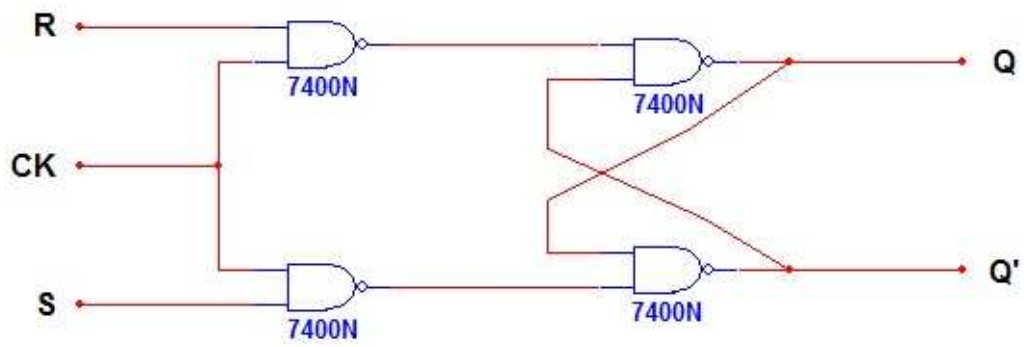


Fig (13-2) Clocked RS flip-flop

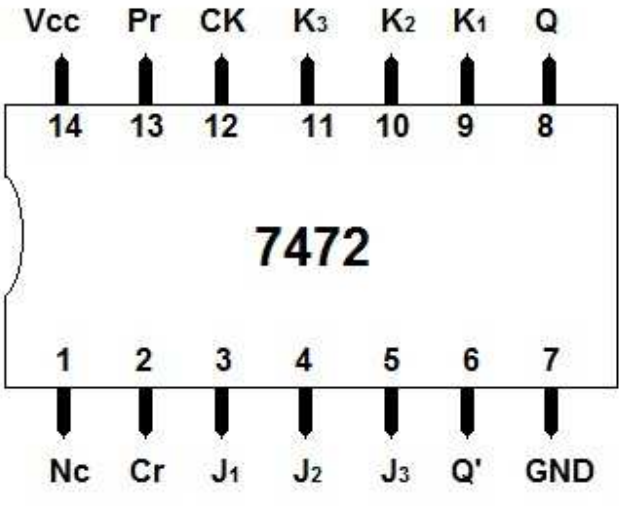


Fig (13-3)a IC7472

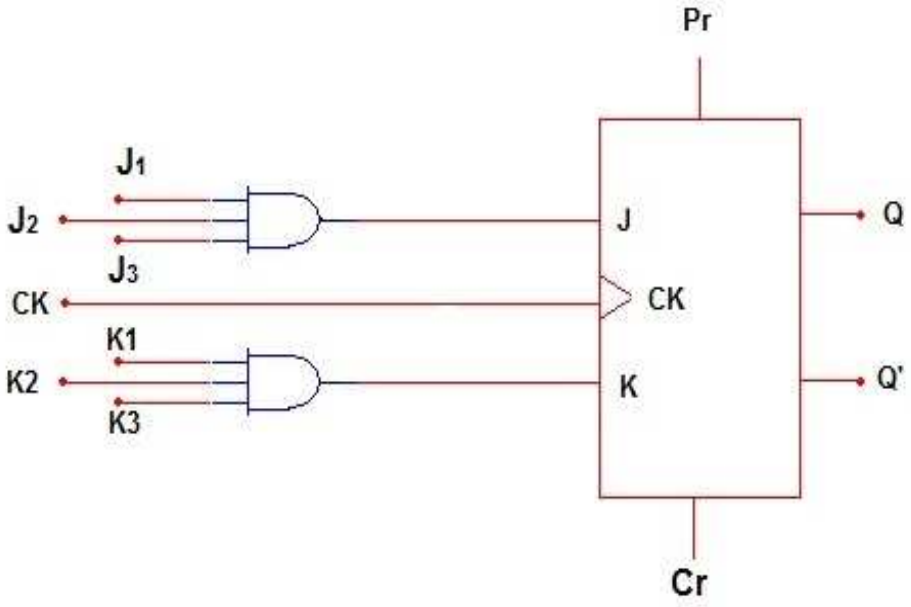


Fig (13-3)b (M/S) JK F-F

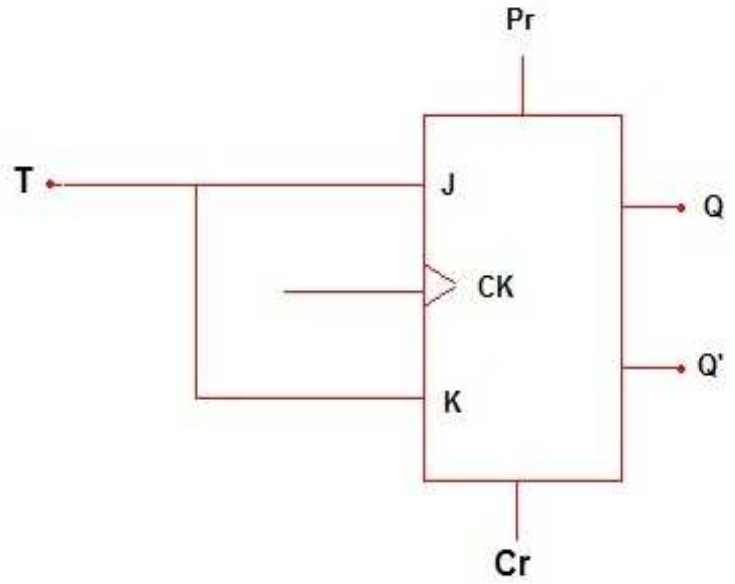


Fig (13-3)c T Flip-Flop

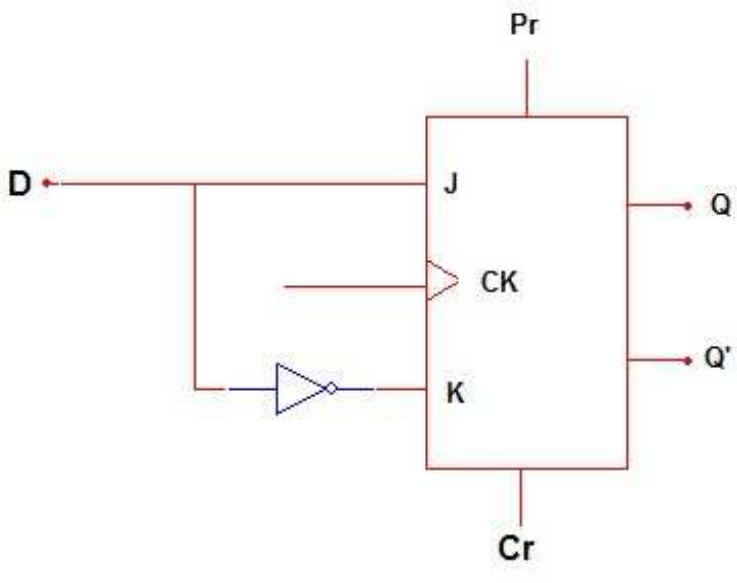


Fig (13-3)d D Flip-Flop

EXPERIMENT NO. (14)
COUNTERS

Introduction:

One common application of sequential logic arrives from the need to count events and time the duration of various processes. These application are called sequential because they follow a predetermines sequence of digital states and are triggered by a timing pulse or clock.

To be useful in digital circuitry and microprocessor system. Counters normally count in binary and can be made to stop or recycle to beginning at any time.

In recycling counter, the number of different binary states defines the modulus (MOD) of the counter.

Flip flop can be used to form binary counters. We can determine the number of different binary output states (modulus) by using the following formula:

Modulus = 2N Where N = number of flip-flops

Asynchronous counters (Ripple counters) means that flip flop is not triggered at exactly the same time.

Synchronous counters can be formed by driving each flip-flop's clock by the same clock input.

Procedure:

A) Up counter :
   1- Connect the MOD -8Ripple counter shown in Fig. (14-1) using M/S-JK flip-flop.
   2- Make Cr = 0 and then 1 to clear the counter.
   3- Write the truth table for 8 clocks (use manual clock).

B) Down counter :
   1- Connect the circuit shown in Fig (14-2).
   2- Repeat steps 2 & 3 in A.

C) Decade counter using 7490 :
   1- Connect MS1 & MS2 TO THE GROUND.
   2- Connect CK to Q0
   3- Clear the counter by making (MR1 &MR2) = 1 and then 0
   4- Write the truth table.

Discussion:

1- What is the difference between Asynchronous and Synchronous counters?
2- Design MOD-8 synchronous counter.

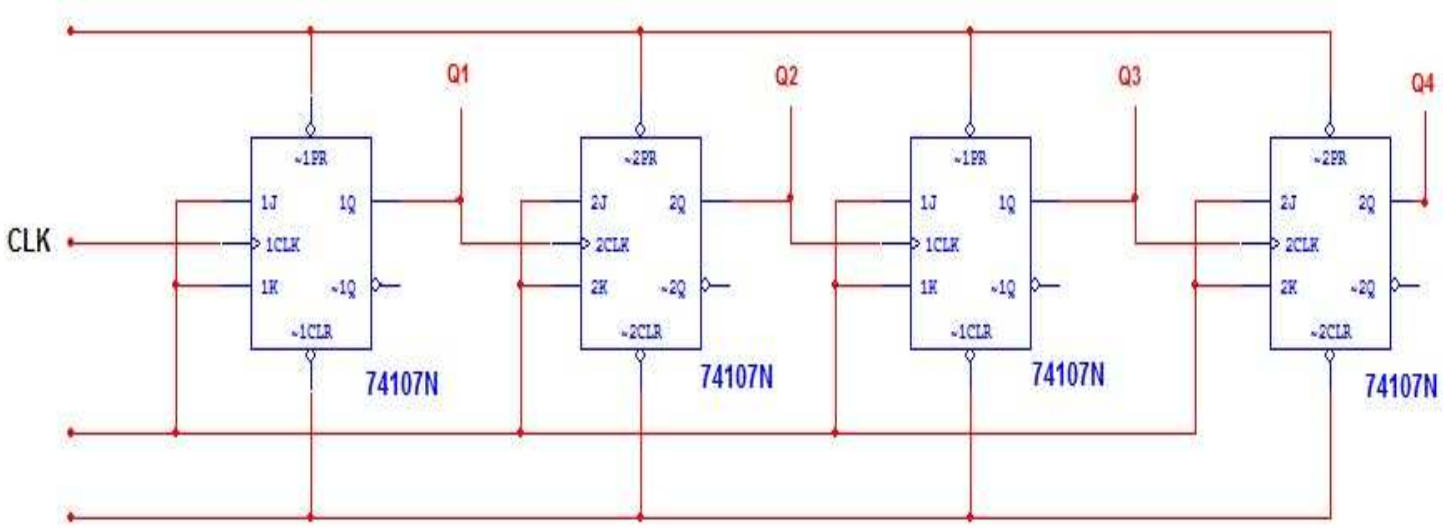


Fig (14-1) Asynchronous UP-Counter

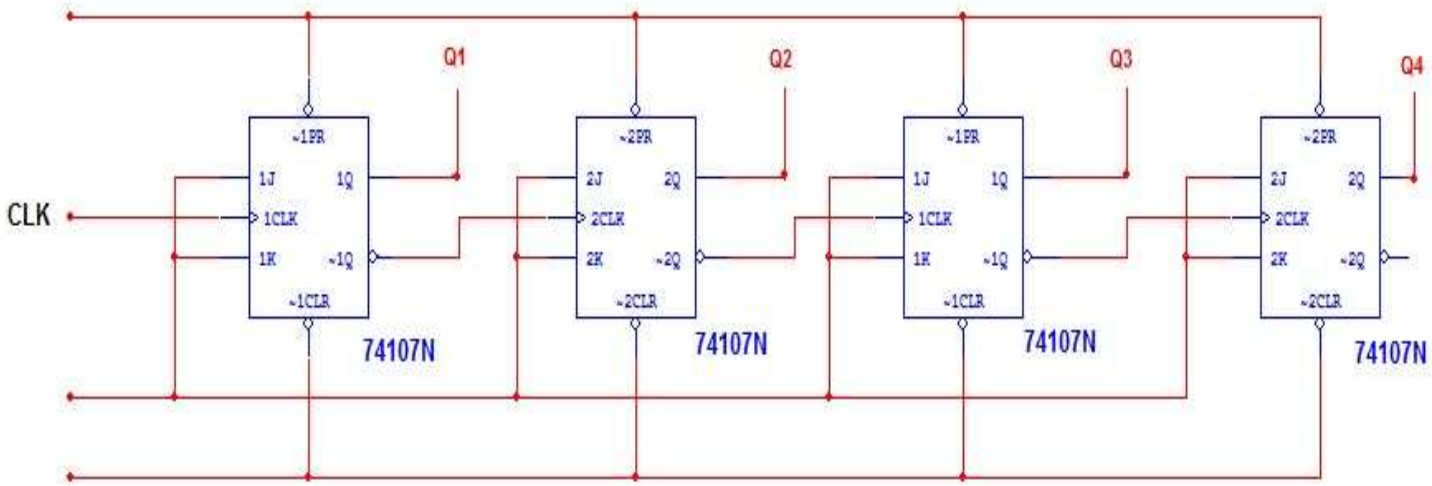


Fig (14-2) Asynchronous Down-Counter

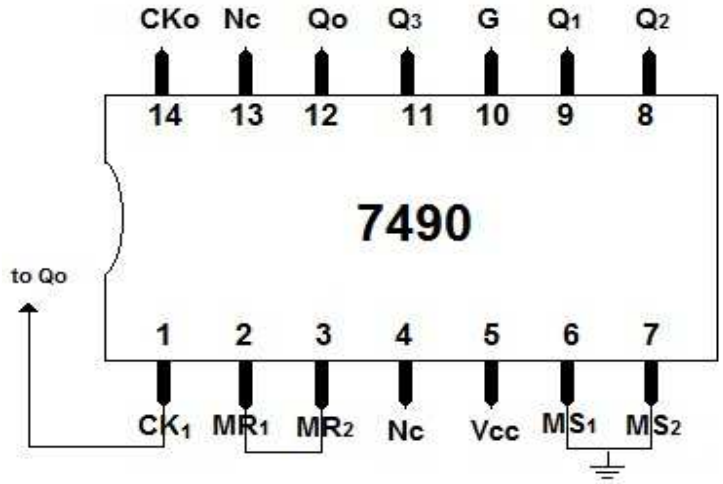


Fig (14-3) 7490 as Decade Counter

EXPERIMENT NO. (15)
MULTIPLEXER & DEMULTIPLEXTER

Objective:

To study the function of multiplexer and de multiplexer circuit.

Theory:

A- Multiplexer (Data Selector):

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to common destination. The basic multiplexer, then has several data input lines and a single output line. It also has data selector inputs that permit digital data on any one of the input to be switched to the output line.

A simple multiplexer can be represented by switch operation that sequentially connects each of the input lines with the output, as illustrated in fig (15-1).

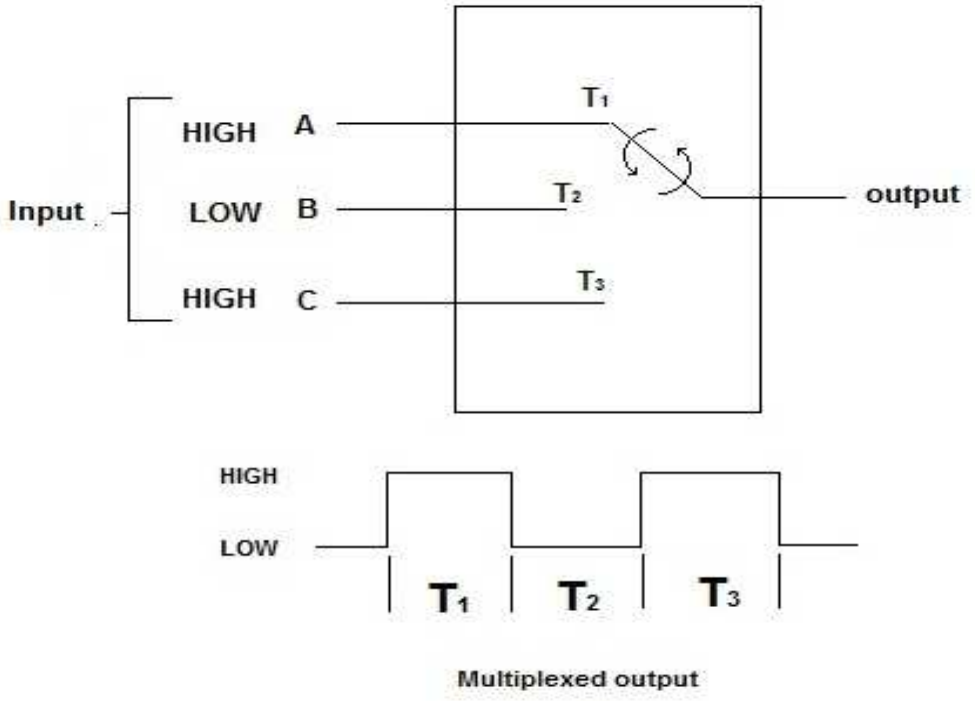


Fig (15-1) Simple Multiplexer operation

Assume that we have logic levels, an indicated on three inputs. During time interval T1, input A is connected to the output; during time interval T2, input B is connected to the output; during time interval T3, input C is connected to the output.

The logic symbol for 4-input multiplexer is shown in fig (15-2).Notice that there are two selection lines because with two selection bits, each of the four data-input lines can be selected.

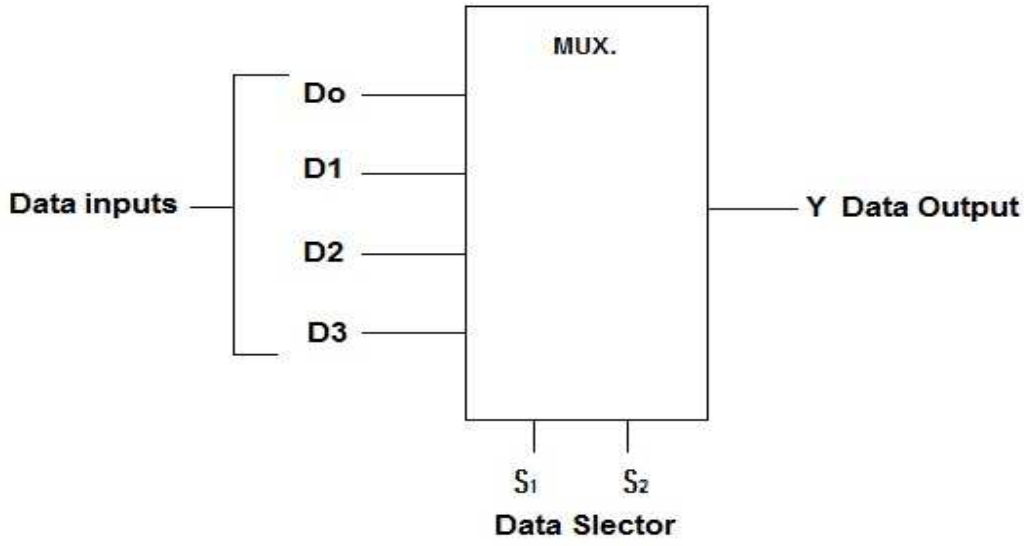


Fig (15-2) Logic symbol for 4-to-1 Data Selector

If a binary 0 (S1 = 0 & So = 0) is applied to the data-select lines, the data on input Do appears on the output. If a binary 1 (S1 = 0 & So = 1) is applied to the data-select lines, the data on input D1 appears on the output. If a binary 2 (S1 = 1 & So = 0) is applied to the data-select lines, the data on input D2 appears on the output. If a binary 3 (S1 = 1 & So = 1) is applied to the data-select lines, the data on input D3 are switched to the output. A summary of this operation is given in table (1).

DATA-SELECT INPUTS		ITNPUT SELECTED
S1	So	
0	0	Do
0	1	D1
1	0	D2
1	1	D3

Table (1) Data Selection for a 4- input Multiplexer.

The data output Y is equal to the data input Do if and only if S1 = 0 and So = 0:
Y= Do S1' So'
The data output Y is equal to the data input D1 if and only if S1 = 0 and So = 1:
Y= Do S1' So
The data output Y is equal to the data input D2 if and only if S1 = 1 and So = 0:
Y= Do S1 So'
The data output Y is equal to the data input D3 if and only if S1 = 1 and So = 1:
Y= Do S1 S2

There terms are (OR), the total expression for the data output is:
Y=Do S1'So'+ Do S1'So+ Do S1 So'+ Do S1So
The implementation of is equation is shown in fig (15-3).

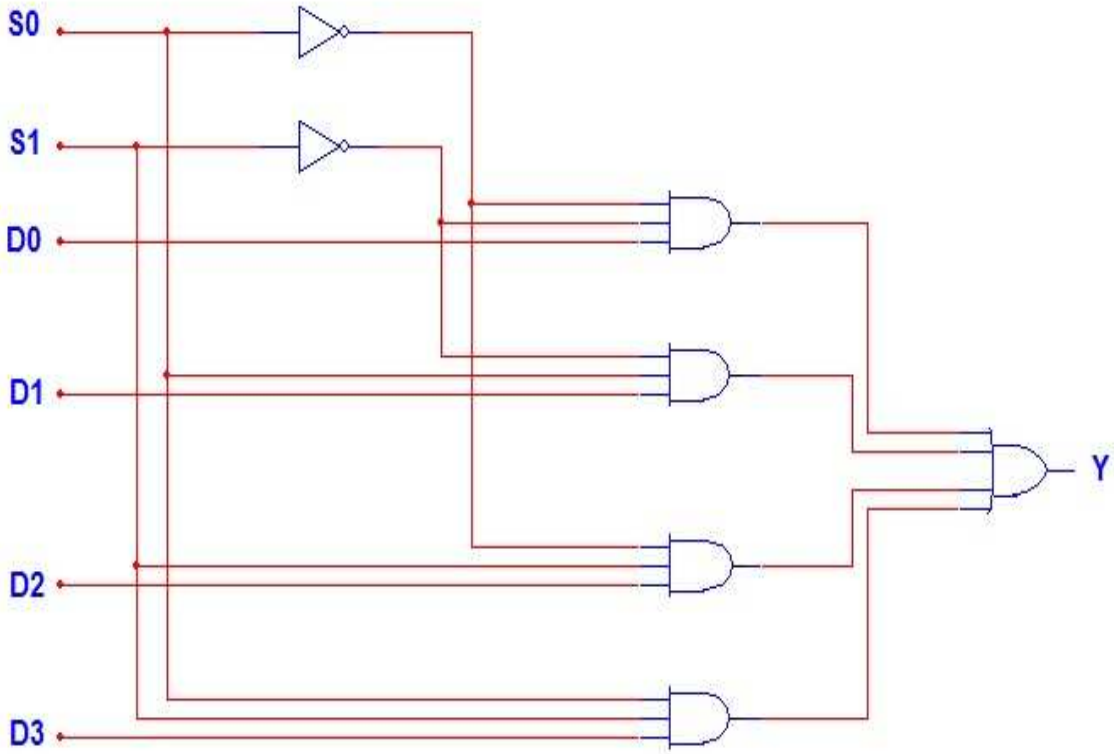


Fig (15-3) Logic Diagram for a 4-input multiplexer

B- Demultiplexer

A demultiplexer (DMUX) basically reverses the multiplexing function. It takes data from one line and distributes them to a given number of output lines. Fig (15-4) shows a one-line to four-line demultiplexer circuit.

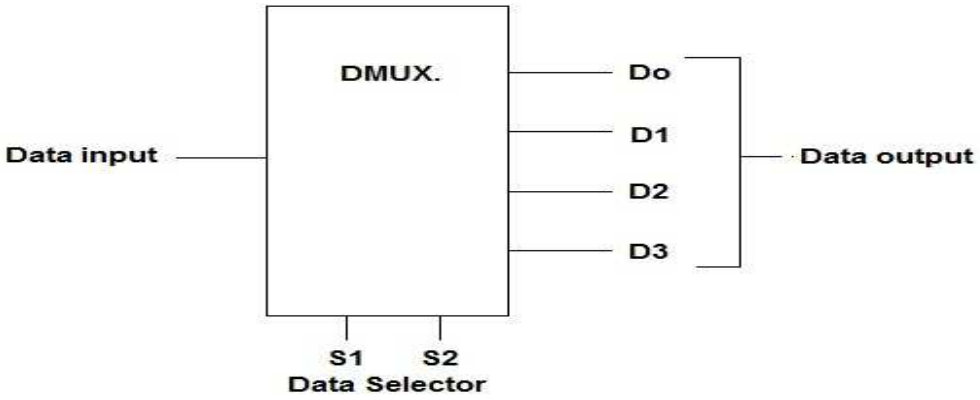


Fig (15-4) Logic Symbol 1-to-4 line demultiplexer

The input data line goes to all of the AND gates. The two select lines will pass through the selected gate to the associated output line.

Fig (15-5) shows a 1-line to 4-line demultiplexer circuit. The two select lines enable only one gate at time, and the data appearing on the input line will pass through the selected gate to the selected gate to the associated output line.

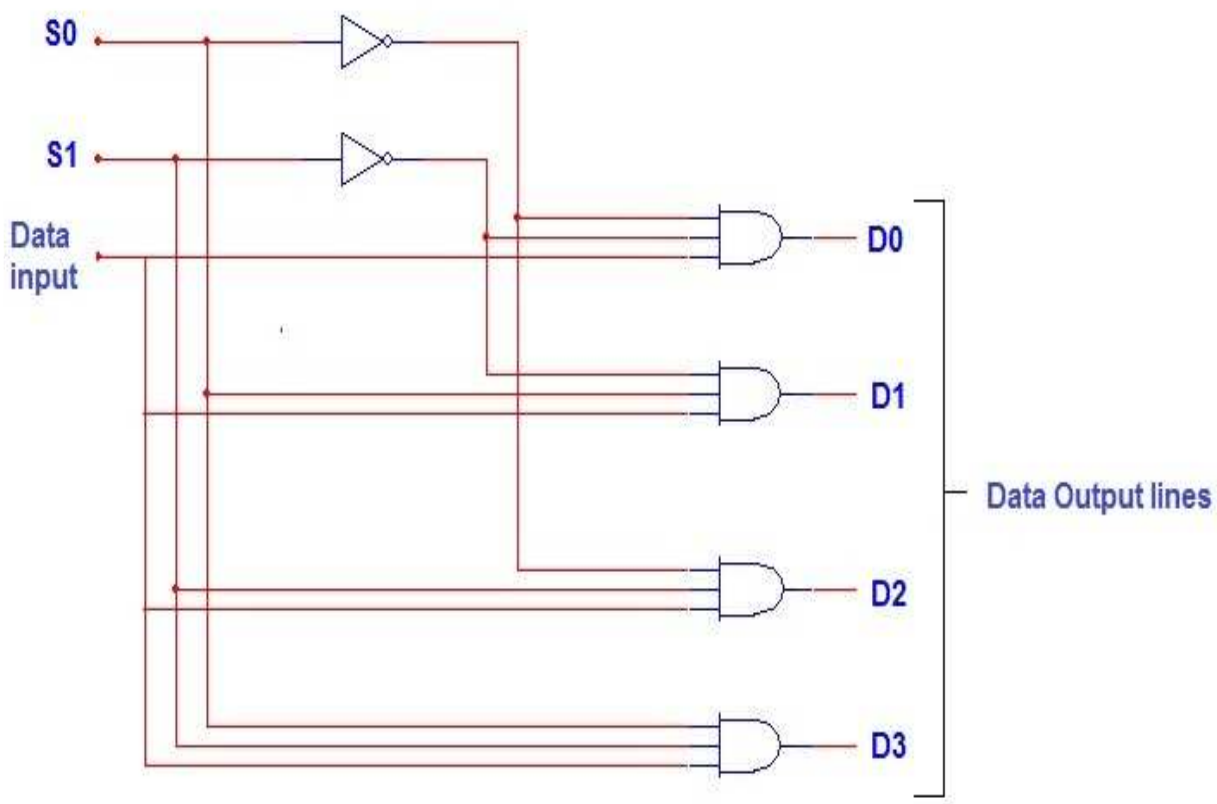


Fig (15-5) 1-to-4 line Demultiplexer

Procedure:

A- Multiplexer:

1- Connect a circuit of 2-to-1 multiplexer and observe its table.

2- Connect a circuit of fig (15-3), and observe its table.

B- Demultiplexer:

Connect a circuit of fig (15-5), and observe its table.

Report:

1- The data input and select waveforms in fig (15-4) are applied to the multiplexer in fig (15-2) Determine the output waveform in relation the input.

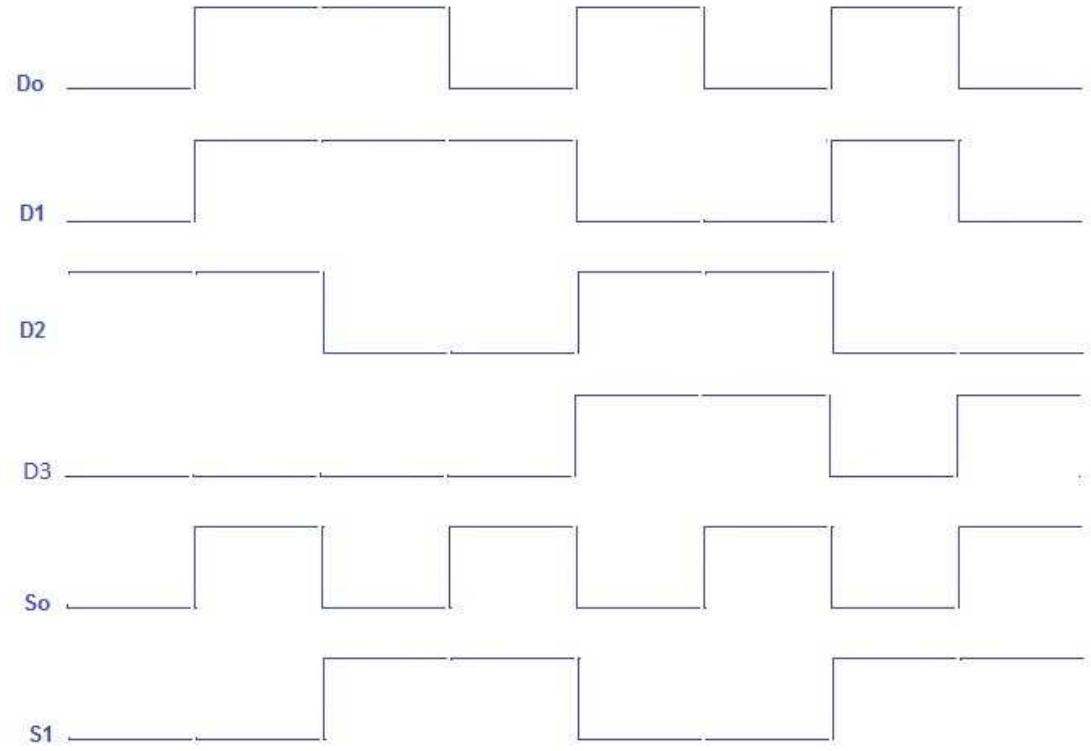


Fig (15-6)

2- The serial data input waveform and data selectors are shown in fig (15-5) determine the data-output waveform for the demultiplexer shown in fig (15-3)

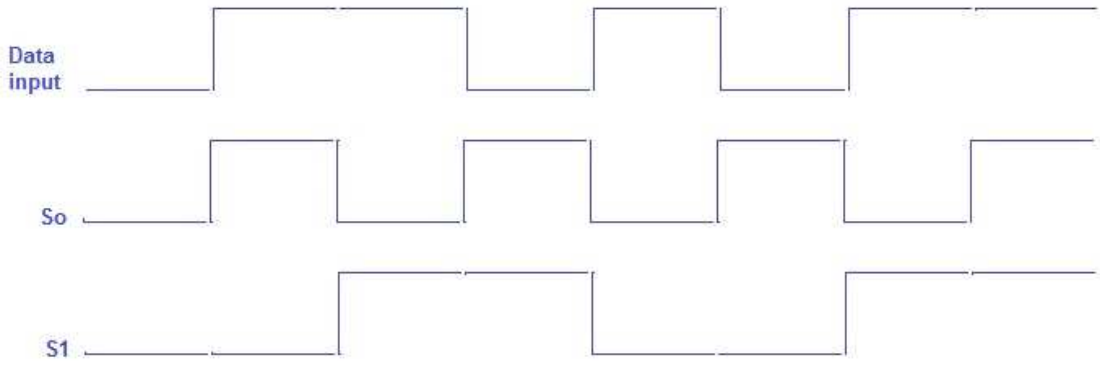


Fig (15-7)

3- Design 6-to-1 MUX. and verify its truth table.
4- Design 1-to-5 DMUX. and verify its truth table.

EXPERMINT NO. (16)
CONSTRACTING BCD ADDER

Objective:

To study the BCD addition circuit.

Theory:

BCD Addition

A 4 bit binary adder (7483) is a nice device for performing binary addition but sometimes we want to decimal addition with binary numbers. In other words we would like.

5+5 =10 (0001 0000)

Instated of

5+5=10 (1010)

To do this we need to generate a carry whenever the sum is greater than 9 and change all letters to the one's digit decimal equivalent (by adding the 0110 <6>).

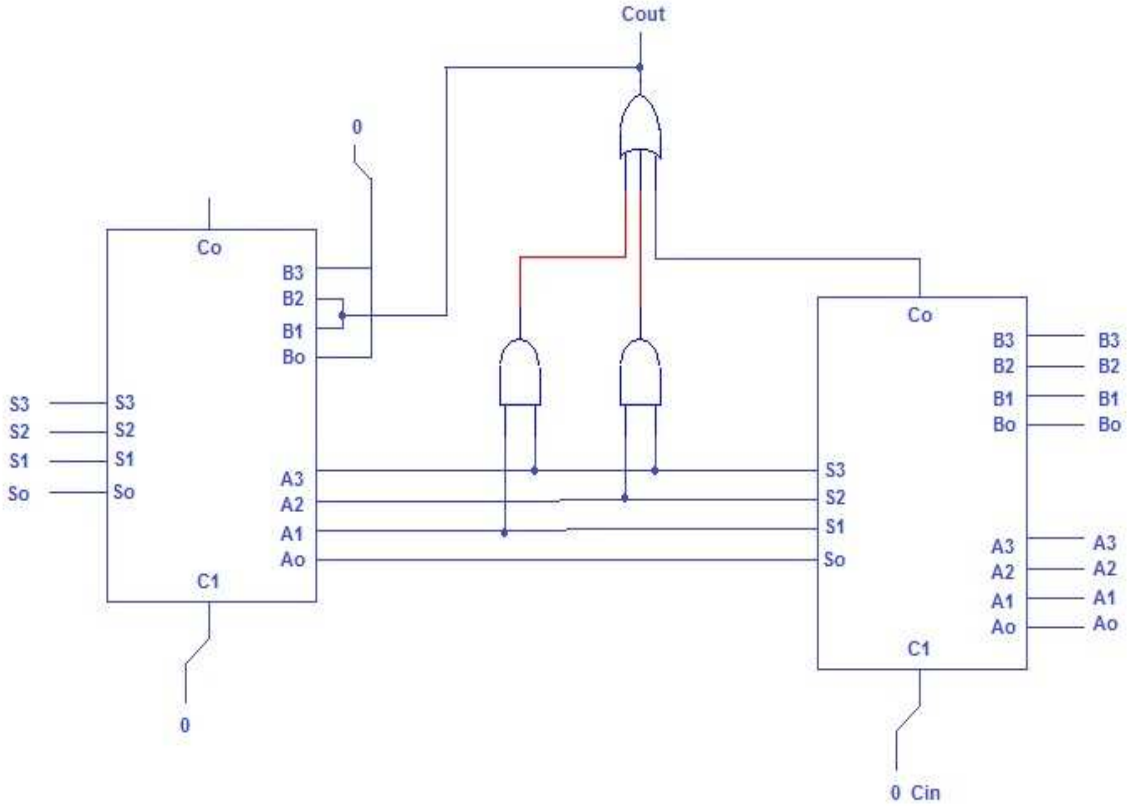


Fig (16-1)

This circuit will do the trick. A carry out is given if the sum is greater than 9. Notice the three inputs to the OR gate.

1- If S<=9, Co of the adder is low and will give us the correct result.
2- If S>=16, Co of the adder is high and will give us our carry.

3- If S=10, 11, 12, 13, 14, 15 then S4,S3 OR S4,S2 will be high so we get the carry for these (from the K-map).

For all switch procedures a carry, we need to adjust the ones digit (the 0110 <6> should be added).

Procedure:

1- Connect the circuit of the figure above.
2- Perform the following addition:
   3+6=9
   5+7=12
   9+9=18

Report:

1- Try to design another circuit for the same purpose.
2- Design a BCD addition circuit using 7483 ICs for addition two numbers each with two digits.

THANKS FOR ALL